basic education

Department:
Basic Education
REPUBLIC OF SOUTH AFRICA

ELECTRICAL TECHNOLOGY (DIGITAL ELECTRONICS)

GUIDELINES FOR PRACTICAL ASSESSMENT TASKS

GRADE 12

2026

These guidelines consist of 46 pages.

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1. INTRODUCTION

The 18 Curriculum and Assessment Policy Statements subjects which contain a practical component all include a practical assessment task (PAT). These subjects are:

- AGRICULTURE: Agricultural Management Practices, Agricultural Technology
- ARTS: Dance Studies, Design, Dramatic Arts, Music, Visual Arts
- SCIENCES: Computer Applications Technology, Information Technology
- SERVICES: Consumer Studies, Hospitality Studies, Tourism
- TECHNOLOGY: Civil Technology, Electrical Technology, Mechanical Technology and Engineering Graphics and Design
- TECHNICAL: Technical Mathematics, Technical Sciences

A practical assessment task (PAT) mark is a compulsory component of the final promotion mark for all candidates offering subjects that have a practical component and counts 25% (100 marks) of the end-of-the-year examination mark. The PAT is implemented across the first three terms of the school year. This is broken down into different phases or a series of smaller activities that make up the PAT. The PAT allows for learners to be assessed on a regular basis during the school year and it also allows for the assessment of skills that cannot be assessed in a written format, e.g. test or examination. It is therefore important that schools ensure that all learners complete the practical assessment tasks within the stipulated period to ensure that learners are resulted at the end of the school year. The planning and execution of the PAT differs from subject to subject.

Practical assessment tasks are designed to develop and demonstrate a learner's ability to integrate a variety of skills in order to solve a problem. The PAT also makes use of a technological process to inform the learner what steps needs to be followed to derive a solution for the problem.

The PAT consists of four simulations and a practical project. The teacher may choose any ONE of the practical projects and any TWO simulations available for DIGITAL ELECTRONICS. For the first simulation to be completed in term 1, the teacher must choose between Simulation 1 and Simulation 2. For Simulation 2 to be completed in term 2, the teacher must choose between Simulation 3 and Simulation 4.

The teacher must apply assessment on an ongoing basis at the same time that the learner is developing the required skills. TWO simulations should be completed by the learners, in addition to the manufacturing of a practical project.

The PAT incorporates all the skills the learner has developed throughout the year. The PAT ensures that all the different skills will be acquired by learners on completion of practical work, as well as the correct use of tools and instruments.

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Requirements for presentation

A learner must present the following:

- PAT file with all the evidence of simulations, design and prototyping. A copy of the PAT 2026 cover page. The relevant simulations and assessment sheets should be copied and handed to each learner to include in the file.
- Practical project with:
  - Enclosure:
    - The file must include a design.
    - The enclosure and the design must match.
    - No cardboard boxes are allowed.
    - Plastic wooden and metal enclosures are acceptable.
    - Enclosures that are manufactured and/or assembled by the learners are preferred.
    - The enclosure should be accessible for scrutiny inside.
    - Lids that are secured are preferred.
  - Circuit board:
    - The file should include the PCB design.
    - The PCB must be mounted inside the enclosure in such a manner that it can be removed for scrutiny. Alternatively, inspection can be made from the bottom in cases where translucent (see-through) enclosures are used.
    - Switches, potentiometers, connectors and other items must be mounted.
    - Wiring must be neat and bound/wrapped.
    - Wiring must be long enough to allow for the PCB to be removed and inspected with ease.
  - Logo and name:
    - The file should contain the logo and name design and specification plate.
    - Logo, specification plate and name must be prominent on the enclosure.
    - The logo/specification plate must be affixed in a permanent manner – painted, glued or stuck on with vinyl.

The PAT will have a financial impact on the school's budget and school management teams are required to make provision for accommodating this particular expense.

PAT components and other items must be acquired timeously, for use by the learners, before the end of the first term at the start of the academic year.

It is the responsibility of the Department Head (DH) to ensure that the teacher is making progress with the PAT from the start of the school year.

Provincial departments are responsible for setting up moderation timetables and consequently PATs should be completed by **31 August 2026**, in time for moderation.

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2. TEACHER GUIDELINES

2.1 How to administer PATs

Teachers must ensure that learners complete the simulations required for each term. The project should be started in January in order to ensure its completion by August. In instances where formal assessments take place, the teacher has to assume the responsibility thereof.

The PAT should be completed during the FIRST THREE TERMS **and must be completed and internally moderated before 31 August 2026. The PAT should be ready for external moderation at the start of PAT moderation programs on 1 September 2026** and must be ready at the start of PAT moderation. Teachers must make copies of the relevant simulations and hand them to learners at the beginning of each term.

The PAT must NOT be allowed to leave the workshop and must be kept in a safe place at all times when learners are not working on them.

The weightings of the PAT must be adhered to and teachers are not allowed to change weightings for the different sections.

2.2 How to mark/assess the PATs

The PAT for Grade 12 will be set and assessed internally, but moderated externally. All formal assessment will be done by the teacher.

The teacher is required to produce a working model and model answer file that sets the baseline for assessment at a Highly Competent Level for every project choice exercised by the learners. This file must include all the simulations with answers the teacher has done him/herself. The teacher will use the model answers and project to assess the simulations and projects of the learners.

Once a facet sheet has been completed by the teacher, assessment will be deemed to be complete. No reassessment will be done once the facet sheets have been completed and captured by the teacher. Learners must ensure that the work is done to the required standard before the teacher finally assesses the PAT during each stage of completion.

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2.3 PAT Programme of Assessment (PAT PoA)

The programme of assessment (PoA) of the PAT is as follows:

TIME FRAME	ACTIVITY	RESPONSIBILITY
	Preparation for PAT 2026	Teacher – Builds the models and works out the model answers for the simulations. Identifies shortages in tools, equipment and consumable items for simulations that must be procured. SMT – Receives procurement requests from teachers and processes payments for the acquisition of required items
January–March 2026	Simulation 1	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations DH – Checks if tasks have been completed and marked by the teacher before the holidays
January 2026	PAT project – procurement	Teacher – Obtains quotations for PAT projects Principal – Approves PAT procurement for PAT projects Teacher – Ensures that PAT projects are ordered and delivered DH – Checks in on teacher to see if the process is adhered to
February- March 2026	PAT project – learners commence with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and collects PAT projects Teacher – Hands out copies of Section B, Design and Make: Part 1 Teacher – Includes practical sessions for learners to complete the PAT project every week Learners - Insert copies of Section B, Design and Make: Part 1 in the PAT file. Complete Section B, Design and Make: Part 1 (Circuit diagram, component list, Description of operation). Teacher – Assesses Section B, Design and Make: Part 1 DH – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
April–June 2026	Simulation 2	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations Learners – Complete Section B, Design and Make: Part 1 (Circuit Board Manufacturing) Teacher – Assesses Section B, Design and Make: Part 1 DH – Checks if tasks have been completed and marked by the teacher before the holidays
April–June 2026	Moderation of Simulation 1	District subject facilitator/subject specialist will visit the school and moderate Simulation 1 10% of learners' work is moderated
April–June 2026	PAT project – learners continue with project	Teacher – Includes practical sessions every week for learners to complete the PAT project Learners – Continue with completion of the PAT project DH – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
July holidays 2026	PAT intervention	Learners that are behind on the PAT are required to complete the project during these holidays
July–August 2026	Moderation of Simulation 2	District subject facilitator/subject specialist will visit the school and moderate Simulation 2 – different learners from the previous term 10% of learners' work is moderated

TIME FRAME	ACTIVITY	RESPONSIBILITY
July–August 2026	PAT project – completion	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out Section B, Design and Make: Part 2 Learners – Insert copies of Section B, Design and Make: Part 2 in the PAT file; complete Section B, Design and Make: Part 2 Teacher – Assesses Section B, Design and Make: Part 2. Transfer marks onto working marksheet DH – Checks to see that 100% of the PAT files and projects are completed and assessed
September 2026	PAT moderation	PAT projects are moderated by subject facilitators/subject specialists from the province and learners are available to demonstrate skills 10% of learners are moderated randomly
October 2026	PAT moderation	PAT projects and simulations are moderated by subject facilitators/specialists from DBE and learners are available to demonstrate skills Learners are moderated randomly

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2.4 Moderation of PATs

Provincial moderation of each term's simulations will start as early as the following term. Simulation 1 should be moderated as soon as the second term starts. Similarly, Simulation 2 will be moderated in July. The project will, however, only be moderated on completion.

During moderation of the PAT, the learner's file and project must be presented to the moderator.

The moderation process is as follows:

- During moderation, learners are randomly selected to demonstrate the different simulations. All four simulations will be moderated.
- The teacher is required to build an exemplar model of each project type chosen for the school.
- This model must be on display during moderation.
- The teacher's model forms the standard of the moderation at Level 4 (Highly Competent).
- Level 5 assessments must exceed the model of the teacher in skill and finishing.
- Learners who are moderated will have access to their files during moderation and may refer to the simulations they completed earlier in the year.
- Learners may NOT ask assistance from other learners during moderation.
- All projects and files must be on display for the moderator.
- If a learner is unable to repeat the simulation or cannot produce a working circuit during moderation, marks will be deducted and circuits assessed as not being operational.
- The moderator will randomly select no fewer than two projects (not simulations) and the learners involved will have to explain how the project was manufactured.
- Where required, the moderator should be able to call on the learner to explain the function and principles of operation, and request the learner to exhibit the skills acquired through the simulations for moderation purposes.
- On completion the moderator will, if needed, adjust the marks of the group upwards or downwards, depending on the outcome of moderation.
- Normal examination protocols for appeals will be adhered to, if a dispute arises from adjustments made.

2.5 Absence/Non-submission of tasks

The absence of a PAT mark in Electrical Technology without a valid reason: The learner will be given three weeks before the commencement of the final end-of-year examination to submit the outstanding task. Should the learner fail to fulfil the outstanding PAT requirement, such a learner will be awarded a zero (0) for that PAT component.

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2.6 Simulations

Simulations are circuits, experiments and tests/tasks which the learner will have to build, test and measure and practically do as part of the development of practical skills. These skills have to be illustrated to the external moderator that visits the school at intervals during the school year.

Teachers who make use of simulation programs on a computer may use them for the learners to practise on. However, it is required that the circuit be built using real components and that measurements be made with actual instruments for the purposes of assessment and moderation.

The correct procedure for completing simulations is outlined below for teachers and school management teams who are responsible for the implementation of the PAT in Electrical Technology.

STEP 1: The teacher will choose **between Simulation 1 and 2 for term 1 and between Simulation 3 and 4 for term 2** from the simulations that are provided.
STEP 2: Compile a list of the components needed for every simulation. Add extra components as these items are very small and you will need extras, as these items get lost/damaged very easily when learners work on them.
STEP 3: Contact three different electronics component suppliers for comparative quotations.
STEP 4: Submit the quotations to the SMT for approval and procurement of the items.
STEP 5: Place the components in storage. Collate items for each simulation, thus making it easier to distribute and use during practical sessions. Ensure that different values of components do not mix, as this would lead to components being used incorrectly and this could damage the component and in extreme cases, the equipment used.
STEP 6: Copy the relevant simulations and hand them out to learners at the start of the term.

Teachers are allowed to adjust circuits and component values to suit their environment/resource availability.

Teachers are required to develop a set of model answers in the teacher's file. Moderators will use the teacher's model answers and artefacts when moderating.

2.7 Projects

The projects are construction projects teachers can choose for their learners. These projects are based on proven circuits provided by schools and subject advisors. The projects are based on working prototypes and require careful construction in order for it to operate correctly.

Projects vary in cost and teachers must ensure that the projects chosen to fall within the scope of the school's budget.

Once the teacher has decided on a circuit, he/she must construct the prototype. Thereafter, copies of the provided circuit can be made and distributed to learners. They MUST redraw these circuits in their files correctly.

The description of the operation of the circuits is NOT complete. Learners are required to interrogate the function of the components in the circuit provided. Learners should elaborate on the purpose of components in the circuit. It is recommended that learners investigate similar circuits available on the internet and in the school library or workshop reference books.

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2.8 Working mark sheet

(A working Excel file is provided with this PAT.)

PAT mark sheet		Term 1	Term 2	Project		Total = Term 1 + Term 2 + Project	Mark out of 100	Moderated mark out of 100
No.	Name of Learner	Simulation 1 or 2 50	Simulation 3 or 4 50	Design and Make Part 1 120	Design and Make Part 2 30	250		
1.								
2.								
3.								
4.								
5.								
6.								
7.								
8.								
9.								
10.								
11.								
12.								
13.								
14.								
15.								
	Total							
	Average							

Teacher Name: _____ Principal Name: _____ Moderator Name: _____

Signature: _____ Signature: _____ Signature: _____

Date: _____ Date:_____ Date:_____

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3. LEARNER GUIDELINES

3.1 PAT 2026 COVER PAGE

(Place this page at the front of the PAT.)

Department of Basic Education Grade 12
CAPS for Technical High Schools Practical Assessment Task – Electrical Technology

Time allowed: Terms 1–3 (2026)

Learner Name: _____

Class: _____

School: _____

Specialisation: DIGITAL ELECTRONICS

Complete simulation 1 or 2 in the FIRST TERM and Simulation 3 or 4 in the SECOND TERM.

Project (Write the name of the project): _____

Evidence of moderation:

NOTE:
When the learner evidence selected has been moderated at school level, the table will contain evidence of moderation. Provincial moderators will sign the provincial moderation and only sign if re-moderation is needed.

Moderation	Signature	Date	Signature	Date
School-based				
District moderation				
Provincial moderation			Re-moderation	

Mark allocation

PAT Component	Maximum Mark	Learner Mark	Moderated Mark
Simulation for Term 1	50		
Simulation for Term 2	50		
Design and Make Project – Circuit	120		
Design and Make Project – Enclosure	30		
Total	**250**		

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3.2 Instructions to the learner

- The practical assessment task counts 25% of your final promotion mark.
- All work produced by you must be your own effort. Group work and co-operative work are NOT allowed.
- The practical assessment task must be completed over three terms.
- The PAT file must contain TWO simulations and a practical project.
- Calculations should be clear and include units. Calculations should be rounded off to TWO decimals. SI units should be used.
- Circuit diagrams can be hand-drawn or drawn on CAD. NO photocopies or scanned files are allowed.
- Photos are allowed and may be in colour or greyscale. Scanned photos and photocopies are allowed.
- This document must be placed inside your PAT file together with the other evidence.
- Learners with identical photos will be penalised and receive zero for that section.

3.3 Declaration of Authenticity (COMPULSORY)

Declaration:

I _____ (name) herewith declare that the work represented in this evidence is entirely my own effort. I understand that if proven otherwise, my final results may be withheld.

_____ _____
Signature of learner Date

4. SIMULATIONS

4.1 Simulation 1: Semiconductors – Inverting op amp

Name of learner: _____	
Class: _____ Date completed: _____	Mark _____ **50**
Date Assessed: _____ Assessor Signature: _____	
Date Moderated: _____ Moderator Signature: _____	

4.1.1 Purpose:

- To connect an inverting operational amplifier circuit using a 741 IC op amp integrated circuit (IC)
- To display the input and output waveforms on an oscilloscope
- To observe how a change in the value of RF affects the gain and output voltage of the circuit

4.1.2 Required resources:

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer Analogue/Digital oscilloscope (dual trace) Function generator Multimeter Variable DC power supply (split supply) Side cutters Wire stripper Long-nose pliers Breadboard	1 x LM 741 op amp 1 x 10 kΩ for R_{IN} 1 x 22 kΩ for R_F 1 x 47 kΩ 1 x 100 kΩ Connecting wires

4.1.3 **Procedure:**

Connect the circuit on the breadboard as shown in FIGURE 4.1.3.

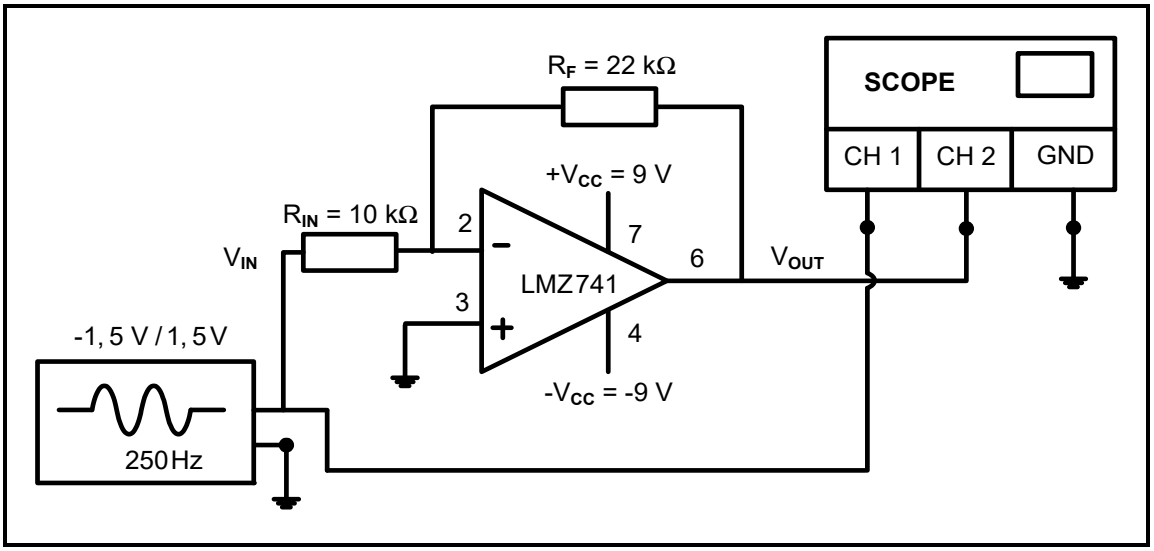
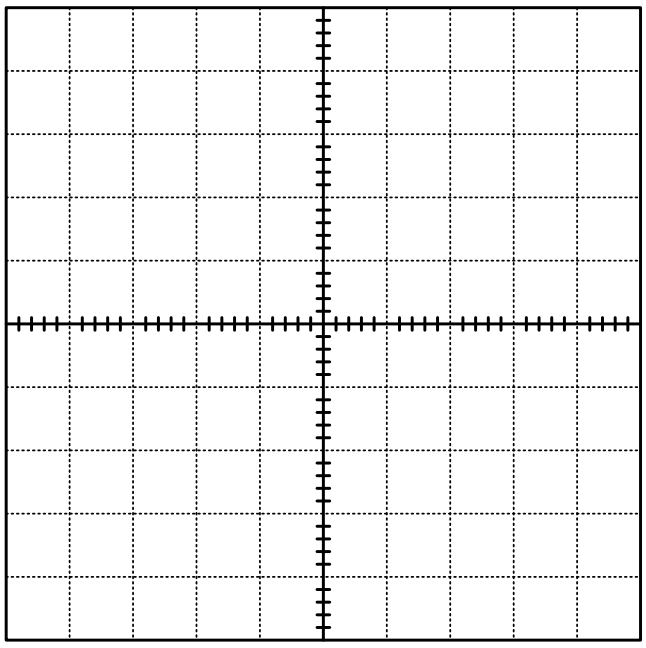


FIGURE 4.1.3 INVERTING OP AMP

4.1.4 Set the oscilloscope up to display at least TWO complete cycles for CH1 and CH2 with the voltage settings to display 2/3rd of the screen.

4.1.5 Draw and label both the input (from CH1) and output (from CH2) waveforms for two complete cycles on the table below.

4.1.6 Write down the peak values of the input and output voltage readings from CH1 and CH2 with R_F = 22 kΩ.



CH 1 V/div: _____

CH 2 V/div: _____

Time/div: _____

V_{IN} :_____

V_{OUT} :_____

NOTE: 1 mark for each correct waveform = 2
1 mark for each oscilloscope setting = 3
1 mark for each voltage measurement = 2

(7)

4.1.7 Use the peak voltage values in 4.1.6 to calculate the gain below.
(All values measured with the oscilloscope are peak values.)

$A_V = -\left(\frac{V_{OUT}}{V_{IN}}\right)$

$A_V =$ _____

= _____

= _____ (2)

4.1.8 Calculate the voltage gain of the circuit by using the resistor as per the circuit diagram in FIGURE 4.1.3.

$A_V =$ _____

= _____

= _____ (3)

4.1.9 Explain the relationship between the input and output waveforms in this circuit configuration with reference to the:

(a) Gain _____
_____ (2)

(b) Amplitude _____
_____ (2)

4.1.10 Measure and record the voltages across V_{OUT} for each R_F change in the table below. Also calculate the voltage gain values in the table below as you change the value of R_1 in the circuit.
Use $A_V = -\left(\frac{V_{OUT}}{V_{IN}}\right)$

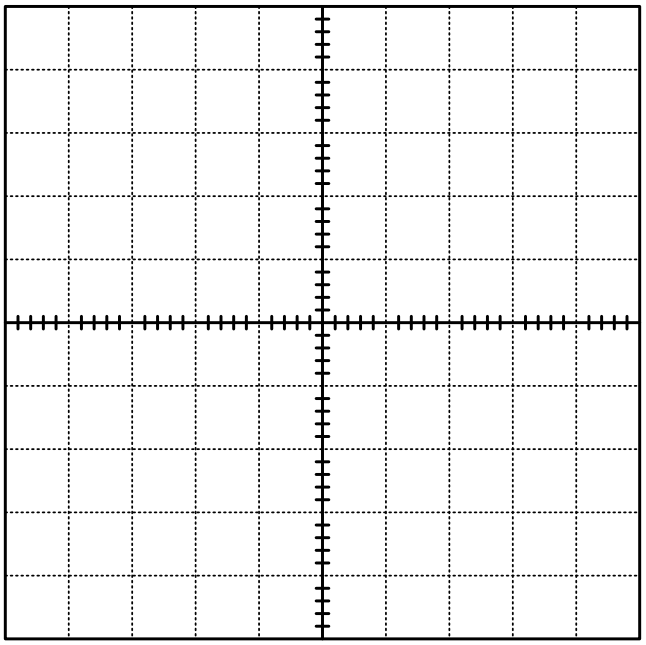
Resistor R_F	V_{OUT}	Formula	Substitution	Voltage gain (A_V)
(a) 10 kΩ	$V_{OUT(1)}$ = _____	$A_V = -\left(\frac{V_{OUT(1)}}{V_{IN}}\right)$	= $-\left(\frac{\quad}{\quad}\right)$	= _____
(b) 47 kΩ	$V_{OUT(2)}$ = _____	$A_V = -\left(\frac{V_{OUT(2)}}{V_{IN}}\right)$	= $-\left(\frac{\quad}{\quad}\right)$	= _____
(c) 100 kΩ	$V_{OUT(3)}$ = _____	$A_V = -\left(\frac{V_{OUT(3)}}{V_{IN}}\right)$	= $-\left(\frac{\quad}{\quad}\right)$	= _____

TABLE: 4.1.10

NOTE: 1 mark for each correct substitution = 3
1 mark for each correct substitution = 3
1 mark for each correct gain calculation = 3

(9)

4.1.11 Draw and label the input and output waveforms for at least two complete cycles in the oscillogram below. Indicate the voltage settings for CH 1 and CH 2 with R_1 = 100 kΩ.



CH 1 V/div: _____

CH 2 V/div: _____

Time/div: _____

V_{IN} : _____

V_{OUT} :_____

NOTE: 1 mark for each correct waveform = 2
1 mark for each oscilloscope setting = 3
1 mark for each voltage measurement = 2 (7)

4.1.12 Calculate the gain of the amplifier by using resistance values when R_F = 100 kΩ.

A_V = _____

= _____

= _____ (3)

4.1.13 Refer to your results in QUESTION 4.1.10 and write a conclusion on your findings:

_____

_____

_____

_____

_____ (5)

Theory: (40)

FACET SHEET FOR SIMULATION 1

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Not yet competent after reassessment of certain/ all parts of the task	**Competent after reassessment of certain parts of the task**	**Competent**	**Outstanding (Highly competent)**	
Building the inverting op amp using LM 741 IC	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes. **(1)**	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes. **(2–3)**	The learner correctly built the circuit without the guidance of the teacher. **(4–5)**	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. **(6)**	$\overline{6}$
Safety aspects	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments. **(0)**	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments **(1)**	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. **(2)**		$\overline{2}$
Attitude/ behaviour/ conduct	The learner was completely reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned /reprimanded. **(0)**	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct, and follow instructional, regulation and workshop practice. **(1)**	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructions, regulation and workshop practice. **(2)**		$\overline{2}$
				Rubric	$\overline{10}$
				Theory	$+\ \overline{40}$
				Total Simulation 1	$=\ \overline{50}$

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4.2 Simulation 2: Switching circuits using a 555 IC

Name of learner: _____	Mark: _____ / **50**
Class: _____ Date completed: _____	
Date Assessed: _____ Assessor Signature: _____	
Date Moderated: _____ Moderator Signature: _____	

4.2.1 Purpose:

- To build/connect an astable multivibrator circuit using a 555 IC on a breadboard, as shown in FIGURE 4.2.3
- To display the output waveforms on an oscilloscope
- To investigate how a change in R_1 and R_2 affects the frequency and duty cycle of the output

4.2.2 Required resources:

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer	1 x 555 IC
Analogue/Digital oscilloscope	1 x 0,1 µF (104) non-polarised
DC power supply (+9 V)	1 x 22 µF (25 V capacitor)
Side cutters	1 x 330 Ω resistor
Wire stripper	1 x 10 kΩ resistor
Long-nose pliers	1 x 47 kΩ resistor
Breadboard	1 x LED
	Connecting wires

4.2.3 Procedure:

Build the circuit in FIGURE 4.2.3 (see next page) on the breadboard.
Connect channel 1 of the oscilloscope across capacitor C_1.
Connect channel 2 of the oscilloscope to pin 3 of the IC.
Switch the circuit ON.
Set the oscilloscope to display at least FOUR complete cycles and observe the output on the oscilloscope. Pay attention to the light from the LED.
Replace resistor R_1 and R_2 as indicated in the simulation question statements.
Answer the questions that follow.

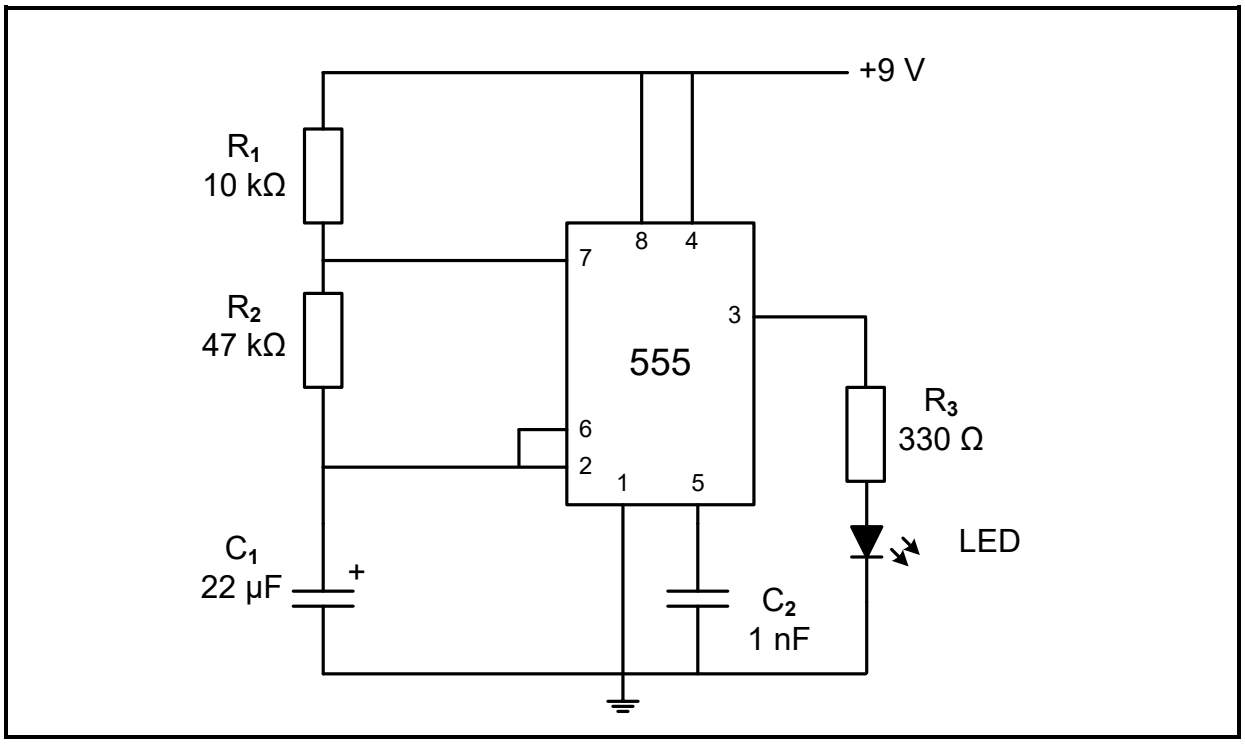
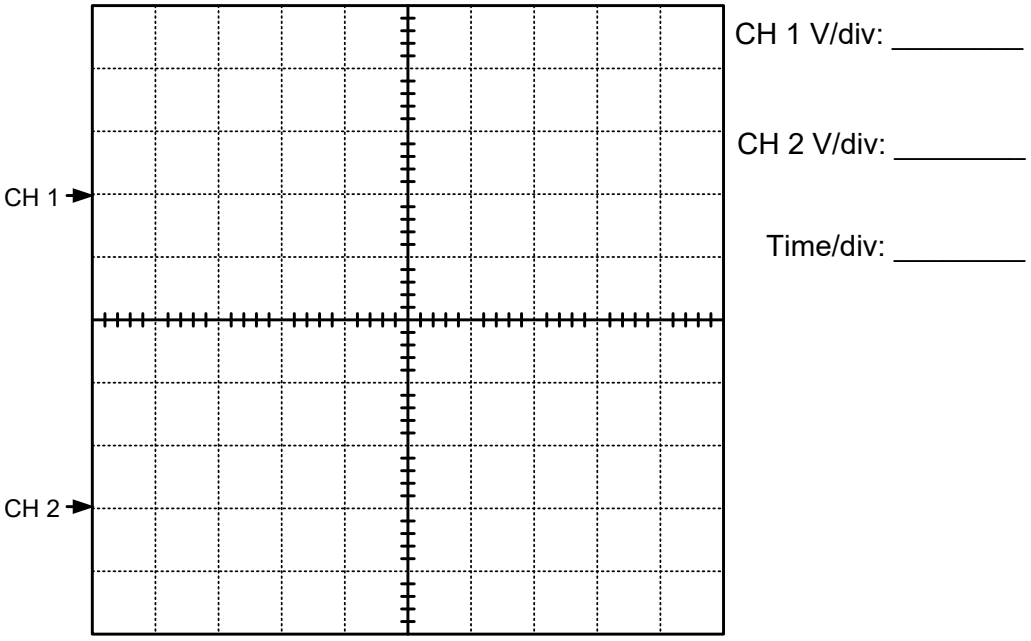


FIGURE 4.2.3: ASTABLE MULTIVIBRATOR CIRCUIT DIAGRAM

PARAMETER	FORMULAE	UNIT
Time high (t_1)	$0,693 \times (R_1+R_2) \times C_1$	Second (s)
Time low (t_2)	$0,693 \times R_2 \times C_1$	Second (s)
Time period (T)	$T = t_1 + t_2$	Second (s)
Frequency (F)	$f = \frac{1}{T}$	Hertz (Hz)
Duty cycle	Duty cycle$= \frac{t_1}{T} \times 100$	Percentage (%)

4.2.4 Set the oscilloscope to display at least four complete cycles of the output waveform with the amplitudes not smaller than two divisions peak-to-peak. Draw the output waveform, when R_1 = 10 kΩ and R_2 = 47 kΩ, on the oscillogram below.



NOTE: 1 mark for two correct waveform cycles when R_1 = 10 kΩ and R_2 = 47 kΩ (2)
1 mark for correct oscilloscope setting (1) (3)

Calculate the following:

(a) The time that the output is high for each half cycle (Time high t_1)

_____
_____
_____
_____ (3)

(b) The time that the output is low for each half cycle (Time low t_2)

_____
_____
_____
_____ (3)

(c) The period of one cycle

_____
_____
_____
_____ (3)

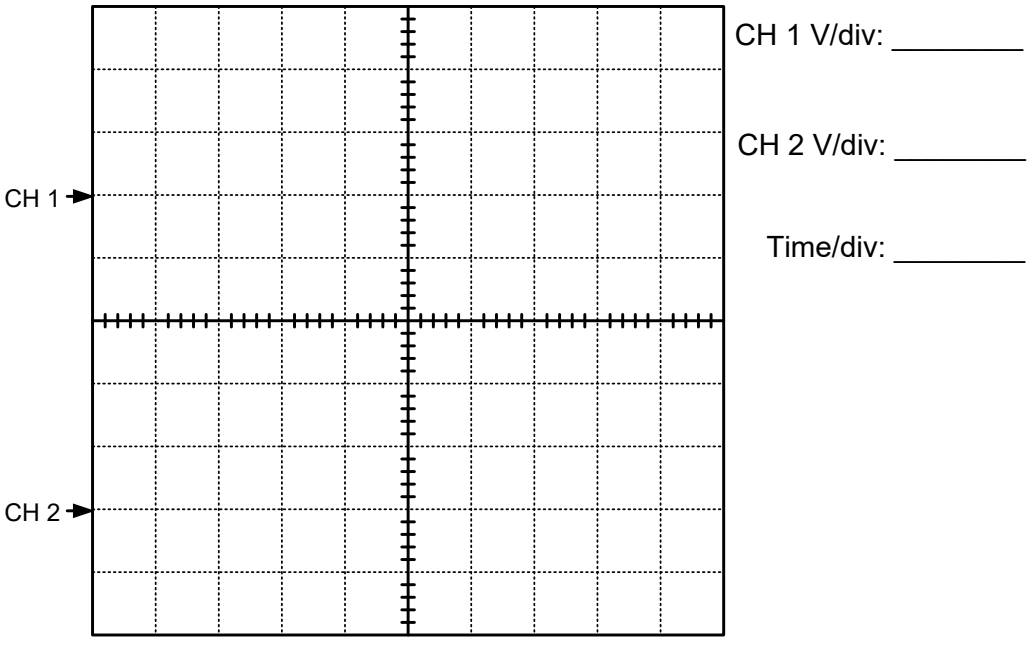
(d) The frequency of the output

_____
_____
_____
_____ (3)

(e) The duty cycle of the waveform

_____
_____
_____
_____ (3)

4.2.5 Set the oscilloscope to display at least four complete cycles of the output waveform with the amplitudes not smaller than two divisions peak-to-peak. Draw the output waveform on the oscillogram below, when R_1 = 47 kΩ and R_2 = 10 kΩ.



NOTE: 2 marks for the correct output waveform when R_1 = 47 kΩ and R_2 = 10 kΩ (2)
1 mark for correct oscilloscope settings (1) (3)

(a) The time that the output is high for each half cycle (Time high $t_{1)}$

_____
_____
_____
_____ (3)

(b) The time that the output is low for each half cycle (Time low t_2)

_____
_____
_____
_____ (3)

(c) The period of one cycle

_____
_____
_____
_____ (3)

(d) The frequency of the output

_____
_____
_____
_____ (3)

(e) Calculate the duty cycle of the waveform.

_____
_____
_____
_____ (3)

4.2.6 Pay careful attention to the voltage across capacitor C_1 and the LED or the output signal displayed by channel 2 of the oscilloscope. Refer to the voltage across the capacitor and explain when the output changes states.

_____
_____
_____ (2)

4.2.7 Refer to C_1, R_1 and R_2 and explain why the duty cycle in 4.2.4 is different from the duty cycle in 4.2.5.

_____
_____
_____ (2)

Simulation 2 (40)

FACET SHEET FOR SIMULATION 2

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Not yet competent after reassessment of certain/all parts of the task	**Competent after reassessment of certain/ all parts of the task**	**Competent**	**Outstanding (Highly competent)**	
Building the astable multivibrator using a 555 IC	The learner was given opportunities to rebuild more than 50% of the circuit after the teacher intervened in identifying and rectifying mistakes. **(1)**	The learner was given an opportunity to rebuild less than 50% of the circuit after the teacher intervened in identifying and rectifying a few mistakes. **(2–3)**	The learner correctly built the circuit without the guidance of the teacher. **(4–5)**	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. **(6)**	$\overline{6}$
Safety aspects	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments. **(0)**	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments. **(1)**	The learner applied safety rules, regulation, and correct procedure when using tools and instruments to wire the circuits without been reminded by the teacher. **(2)**		$\overline{2}$
Attitude/ Behaviour Conduct	The learner was completely reluctant to work, cooperate, take responsibility of their own conduct and follow instructional regulation and workshop practice even after being cautioned/ reprimanded. **(0)**	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct, and follow instructional, regulation and workshop practice **(1)**	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct, and follow instructions, regulation and workshop practice. **(2)**		$\overline{2}$
				Rubric	$\overline{10}$
				Theory	$+\ \overline{40}$
				Total Simulation 2	$=\ \overline{30}$

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4.3 Simulation 3A: Full adder circuit

Name of learner: _____	Mark _____
Class: _____ Date completed: _____	**50**
Date Assessed: _____ Assessor Signature: _____	
Date Moderated: _____ Moderator Signature: _____	

4.3.1 Purpose:

- To connect the circuit on the breadboard
- To demonstrate the operation of the full adder
- To observe the change in the outputs (LED_1 and LED_2) when input switches S_1, S_2 and S_3 are pressed

4.3.2 Required resources:

TOOLS/INSTRUMENTS	MATERIALS
Breadboard Voltmeter Power supply 5 V Side cutters	74LS86 IC (XOR gate) 74LS08 IC (AND gate) 74LS32 IC (OR gate) Toggle switches x 3 220 Ω resistor x 2 10 kΩ resistor x 3 1 x red and 1 x green LED Connecting wires

4.3.3 Procedure:

Refer to FIGURE 4.3.3(a) below and complete a full adder circuit on FIGURE 4.3.3(b).

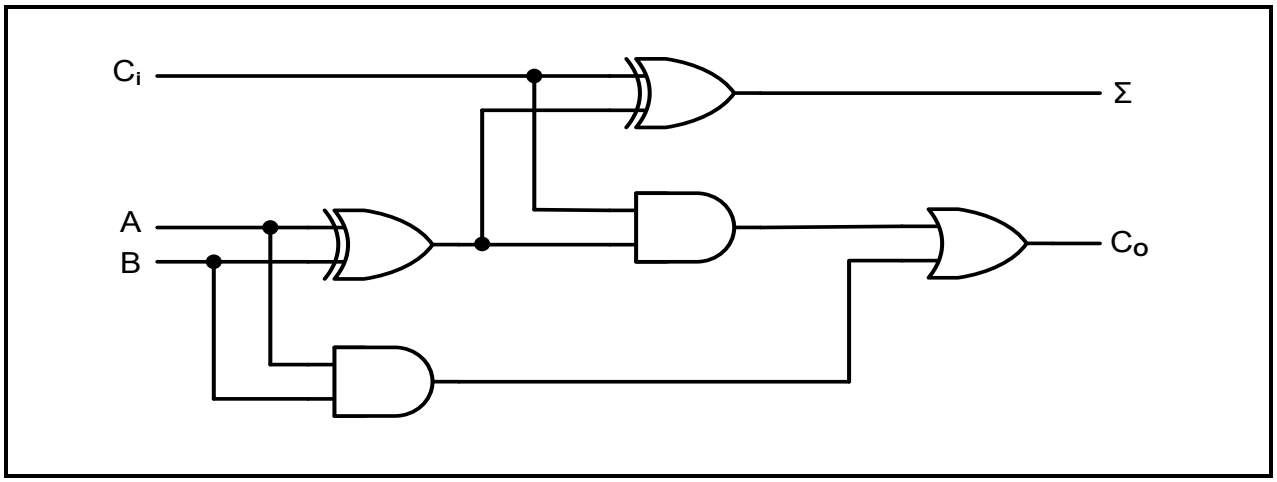


FIGURE 4.3.3(a)

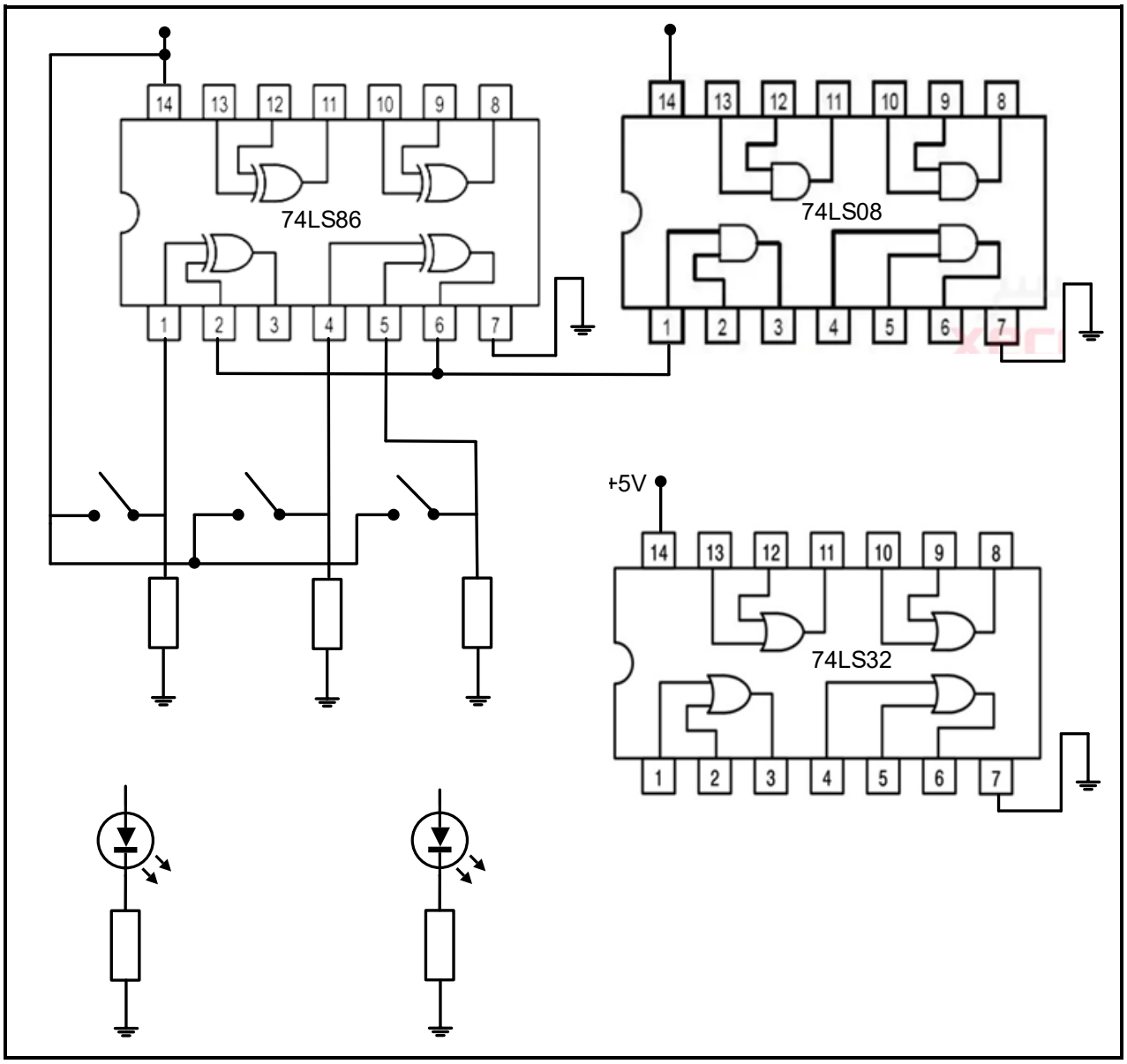


FIGURE 4.3.3(b)

NOTE: 1 mark for each correctly connected LED = 2
1 mark for each correctly connected combination of the XOR gate and the AND gate = 3
1 mark for each correctly output of the AND gate = 2 (7)

4.3.4 Connect the circuit that you have completed above by using a breadboard and then complete the TRUTH TABLE 4.3.4 on the next page.

'0' = SWITCH OPEN
'1' = SWITCH CLOSED
'0' = LED OFF
'1' = LED ON

INPUTS			**OUTPUTS**	
S_1	S_2	S_3	LED_1	LED_2
0	0	0	0	0
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

TABLE 4.3.4 (7)

4.3.5 State ONE application of adders. (1)

Subtotal (15)

FACET SHEET FOR SIMULATION 3A

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Not yet competent after reassessment of certain/all parts of the task	**Competent after reassessment of certain/ all parts of the task**	**Competent**	**Outstanding (Highly competent)**	
Connect/Build the full adder circuit	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes. **(1)**	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes. **(2–3)**	The learner correctly built the circuit without the guidance of the teacher. **(4)**	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. **(5–6)**	$\overline{6}$
Safety aspects	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments. **(0)**	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments. **(1)**	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. **(2)**		$\overline{2}$
Attitude/ Behaviour/ Conduct	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/ reprimanded. **(0)**	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. **(1–2)**	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. **(3)**		$\overline{2}$
				Theory	$\overline{15}$
				Rubric	$+\ \overline{10}$
				Total Simulation 3A	$=\ \overline{25}$

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4.3 Simulation 3B: Connecting an up counter using 74LS76 Dual J-K Flip-flops IC

Name of learner: _____	
Class: _____ Date completed: _____	Mark _____ **50**
Date Assessed: _____ Assessor Signature: _____	
Date Moderated: _____ Moderator Signature: _____	

4.3.6 **Purpose:**

To build/connect an up counter using J-K flip-flops

4.3.7 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Multimeter Side cutters Wire stripper	LD-2 logic designer OR breadboard 74LS76 dual J-K flip-flops with set and clear Jumper wires TTL data book Power supply 5 V

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4.3.8 **Circuit diagram**

Procedure:

Connect the circuit diagram shown in FIGURE 4.3.8(a) below.
Use extra caution when wiring the power and ground connections.
Press PB1 to reset the counter.

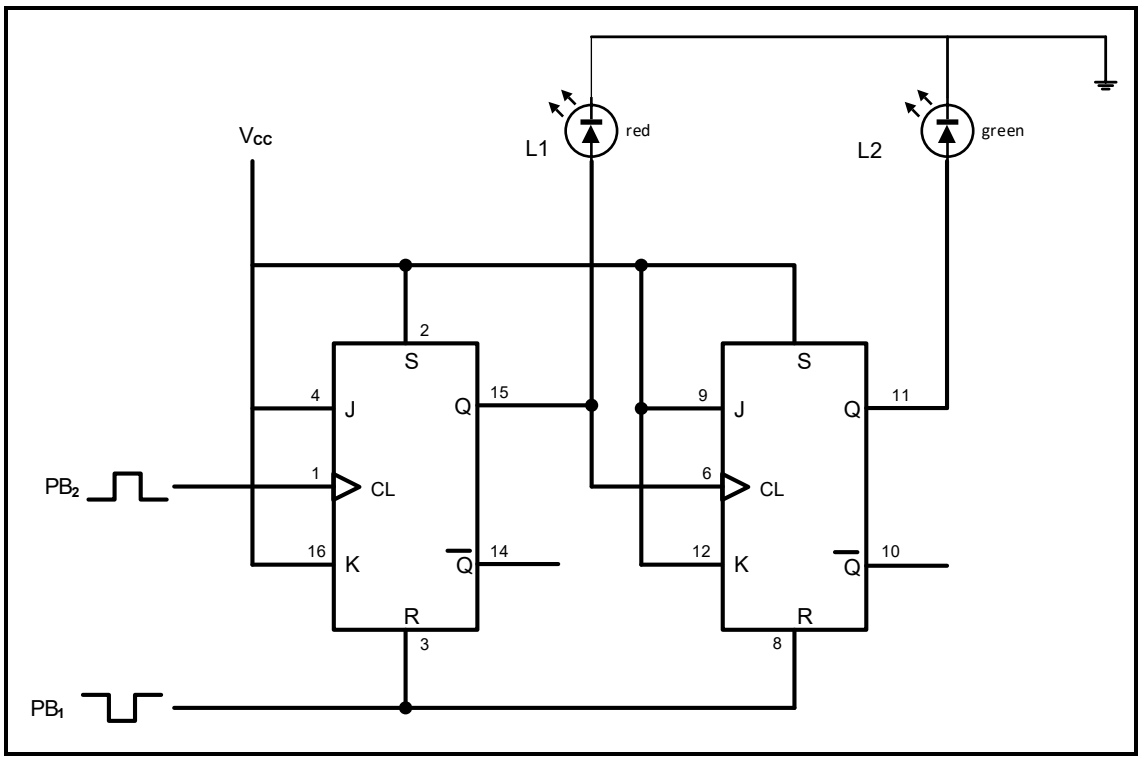


FIGURE 4.3.8(a): CIRCUIT DIAGRAM OF AN UP COUNTER USING J-K FLIP-FLOPS

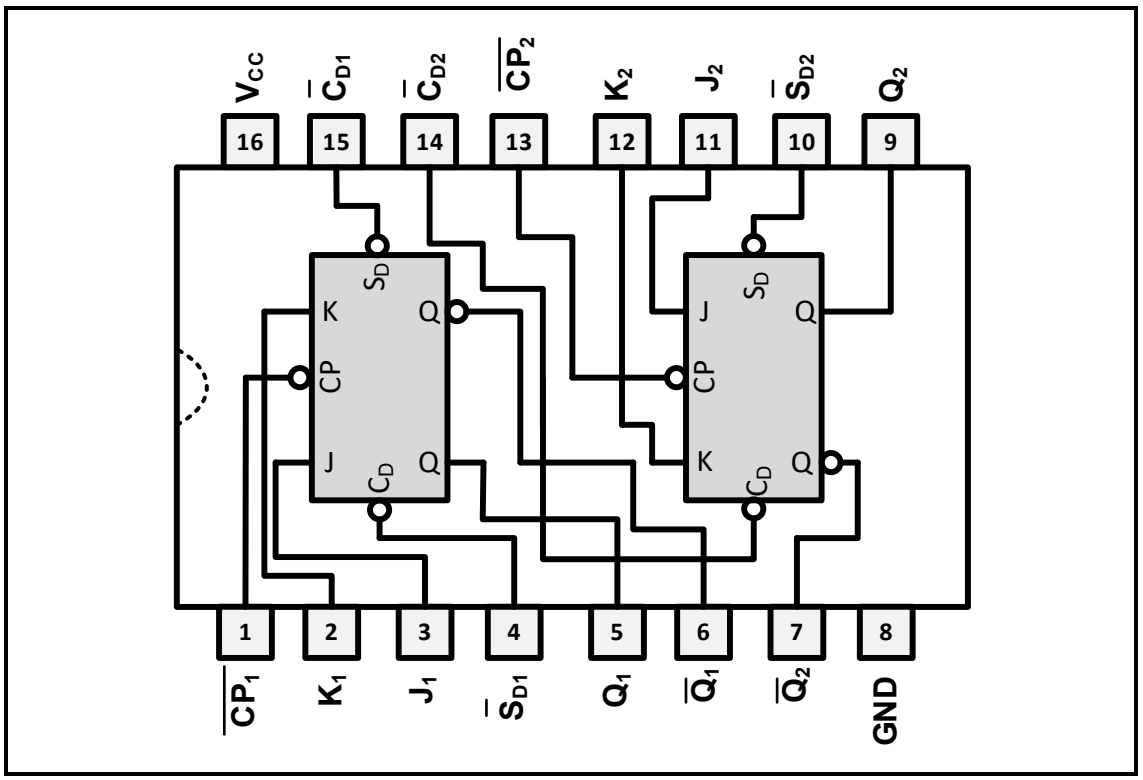


FIGURE 4.3.8(b): PIN LAYOUT OF THE 74LS76 IC

4.3.9 **Procedure and observation:**

(a) Turn on the power to the circuit. Press PB1. **NOTE:** All lights should be AF.

Press switch PB_2 repeatedly and complete TABLE 4.3.9 below by writing the state of the outputs of LEDs L1 and L2.

'0' = LED OFF
'1' = LED ON

PB_2	L1	L2
1		
2		
3		
4		
5		

TABLE 4.3.9

(5)

(b) Observe the output state of L1 and L2 in row 4 and 5 and write your conclusion about the operational sequence of the counter.

_____

_____

_____ (2)

(c) Determine the highest number the count can display.

_____ (1)

(d) Refer to TABLE 4.3.9 above and complete the timing diagram in FIGURE 4.3.9 below.

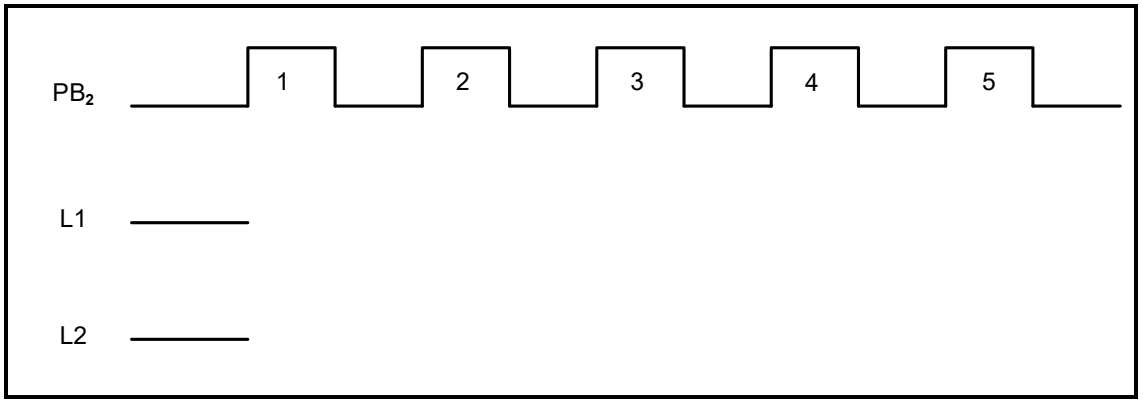


FIGURE 4.3.9

(5)
(13)

4.3.10 **Housekeeping**

When you have obtained all the measurements and the teacher has validated all your answers, you must tidy up your workplace as part of the safety in the workshop. You will be assessed on housekeeping with the rubric on the next page.

FACET SHEET FOR SIMULATION 3B

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Not yet competent after reassessment of certain/all parts of the task	**Competent after reassessment of certain/ all parts of the task**	**Competent**	**Outstanding (Highly competent)**	
Connecting/ building the up counter using J-K flip- flop circuit	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes. **(1)**	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes. **(2–3)**	The learner correctly built the circuit without the guidance of the teacher. **(4)**	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. **(5–6)**	$\overline{6}$
Safety aspects	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments. **(1)**	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments. **(2)**	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. **(3)**		$\overline{3}$
Attitude/ Behaviour/ Conduct	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/reprimanded. **(0)**	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. **(1–2)**	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. **(3)**		$\overline{3}$
				Rubric	$\overline{12}$
				Theory	$+\ \overline{13}$
				Total Simulation 3A	$=\ \overline{25}$
				Total Simulation 3B	$=\ \overline{25}$
				TOTAL:	$=\overline{50}$

4.4 Simulation 4A: Connecting a 7-segment display to a 4-bit BCD 7-segment driver

Name of learner: _____	Mark _____
Class: _____ Date completed: _____	**50**
Date Assessed: _____ Assessor Signature: _____	
Date Moderated: _____ Moderator Signature: _____	

4.4.1 Purpose:

- To build a 7-segment display connected to a 4-bit BCD 7-segment display driver
- To observe the output on the 7-segment display after powering up the circuit

4.4.2 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer Breadboard Variable DC power supply Side cutters Breadboard wire	CD4511 IC CD4518B IC 7-segment display R_1- R_8 = 10 kΩ R_9 – R_{19} = 470 kΩ C_1 = 22 µF LEDs x 4, in different colours

4.4.3 **Activity 4.4A**

Connect the circuit below on a breadboard and observe the output.

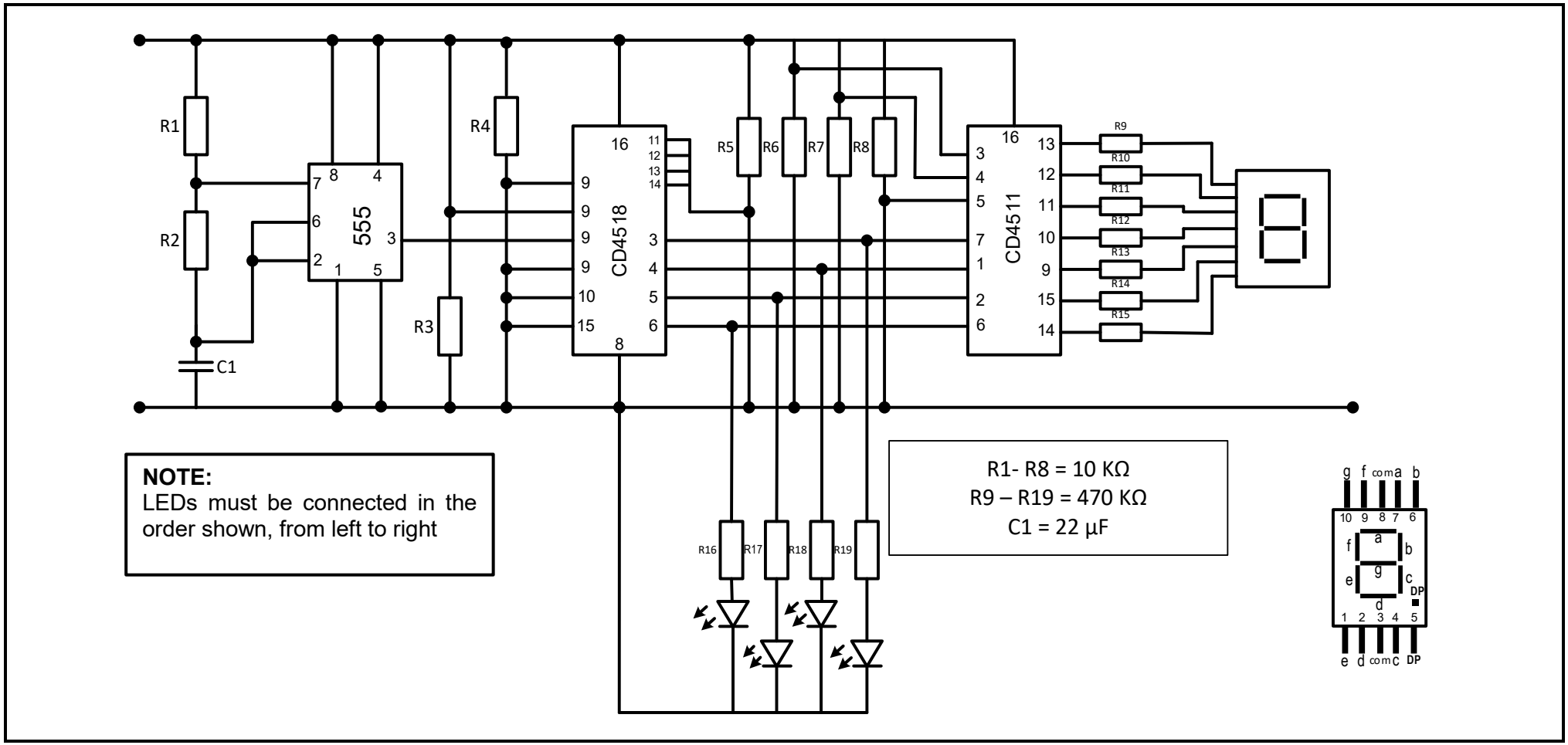


FIGURE 4.4.3: CIRCUIT DIAGRAM OF 7-SEGMENT DISPLAY CONNECTED TO A 4-BIT BCD 7-SEGMENT DRIVER

4.4.4 When you have obtained all the measurements and the teacher has validated all your answers, you must tidy up your workplace as part of safety in the workshop. You will be assessed on housekeeping with the rubric on the next page.

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FACET SHEET FOR SIMULATION 4A

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Not yet competent after reassessment of certain parts of the task	**Competent after reassessment of certain/all parts of the task**	**Competent**	**Outstanding (Highly competent)**	
Connecting the 7-segment display to a 4-bit BCD 7-segment display driver	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes. **(1)**	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes. **(2)**	The learner correctly built the circuit without the guidance of the teacher. **(4)**	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. **(6)**	$\overline{6}$
Safety aspects		The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments. **(1)**	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. **(2)**		$\overline{2}$
Hand tools				Used hand tools correctly. **(1)**	$\overline{1}$
Preparation for insertion of components into breadboard		Checked the datasheet on the ICs. **(1)**	Set supply voltage correct at +9 .V **(2)**		$\overline{2}$
Correct connection on breadboard – nodes and polarity	8 nodes for correct connection of CB4518B IC **(4)**	15 nodes for correct connection of CD4511 IC and the 7-segment display **(8)**	20 nodes for correct connection of CD4511 IC and the 7-segment display **(12)**		$\overline{12}$
Attitude/ Behaviour/ Conduct	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/ reprimanded. **(0)**	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. **(1)**	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. **(2)**		$\overline{2}$
				Rubric	$\overline{25}$

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Simulation 4B: PICAXE

4.4.5 **Purpose:**

To test knowledge of flow diagrams and PICAXE

Study the scenario below and design a flow diagram for the PICAXE school parking lot access control system.

SCENARIO:

Your school has limited access for vehicles that enter the school parking lot.

Design and simulate a PICAXE school parking lot control system for 50 vehicles to enter the school lot when a space is available. There will be an entrance and exit on each end of the school parking lot.

This system is set up to have a single entrance and a single exit at the school parking lot.
This system will enable access control for vehicles.
It will consist of a red light and a green light.
The green light informs the vehicle entering the school parking lot that a space is available.
The system will use two digital sensors.
Sensor 1 will increase the count when vehicles enter the school parking lot.
Sensor 2 will decrease the count when vehicles exit the school parking lot.
Sensor 1 will increase the count to 30 vehicles inside the school parking lot and the program will toggle to the red light. This will indicate a full school parking lot.
Sensor 2 will reduce the count when vehicles leave. The green light switches on if the count is less than 30, which indicates that a vehicle may now enter the school parking lot.

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FACET SHEET FOR SIMULATION 4B

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Not yet competent after reassessment of certain/all parts of the task	**Competent after reassessment of certain parts of the task**	**Competent**	**Outstanding (Highly competent)**	
Inserting the Start/Stop element			Either start or stop element correctly placed **(1)**	Both start and stop element correctly placed **(2)**	$\overline{2}$
Inserting the decision element			Two decision elements correctly placed **(1)**	Four decision elements correctly placed **(2)**	$\overline{2}$
Inserting the process element	One process element correctly placed **(1)**		Two process elements correctly placed **(2)**	Three process elements correctly placed **(3)**	$\overline{3}$
Inserting the data elements	One data element correctly placed **(1)**	Two data elements correctly placed **(2)**	Three data elements correctly placed **(3)**	Four data elements correctly placed **(4)**	$\overline{4}$
Inserting the flow lines correctly	0%–25% of flow lines correctly placed **(1–2)**	25%–50% of flow lines correctly placed **(3–4)**	50%–75% of flow lines correctly placed **(5–6)**	All flow lines correctly placed **(7–8)**	$\overline{8}$
Labelling of elements	0–3 labels correctly placed **(1)**	4–6 labels correctly placed **(2–3)**	7–9 labels correctly placed **(4–5)**	All labels correctly placed **(6)**	$\overline{6}$
				Rubric	/25
				Total Simulation 4A	= /25
				Total Simulation 4B	+ /25
				TOTAL:	= /50

5. SECTION B: DESIGN AND MAKE

Design and Make Project

Time: January to August 2026

Learner Name: _____

School: _____

Class: _____

Title/Type of Project: _____

INSTRUCTIONS

- This section is COMPULSORY for all learners.
- The teacher will choose a circuit for the project.
- Any project constructed must include at least (but is not limited to):
  - Seven components
  - A variety of components (both active and passive)
  - PCB making in some form
  - Soldering
  - An enclosure with a switch and protection
- The checklist below must be used to ensure that all the required tasks for the PAT have been completed.

PAT CHECKLIST

The learner MUST fill in this checklist BEFORE marking of the section takes place.

NO.	DESCRIPTION	TICK (☑)	
		NO	YES
Design and Make: Part 1			
1.	Circuit diagram drawn	☐	☐
2.	Circuit description filled in	☐	☐
3.	Component list completed	☐	☐
4.	Tools list for circuitry populated	☐	☐
5.	Measuring instrument list filled in	☐	☐
Design and Make: Part 2			
1.	Enclosure design completed and included in the file	☐	☐
2.	Unique name written down and on the enclosure	☐	☐
3.	Logo designed and on the enclosure	☐	☐
Miscellaneous			
1.	Enclosure included in the project	☐	☐
2.	Enclosure prepared and drilled according to the design	☐	☐
3.	Enclosure finished off and completed with name and logo	☐	☐
4.	PCB securely mounted in the enclosure using acceptable techniques	☐	☐
5.	Circuit inside the enclosure accessible	☐	☐
6.	Internal wiring neat and ready for inspection	☐	☐
7.	File and project completed and ready for moderation at the workshop/room	☐	☐

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5.1 Design and Make: Part 1

5.1.1 Circuit diagram

Draw a circuit diagram of the project chosen and paste it on the next page.

5.1.2 Project: Description of operation

Use the space below to describe how the project operates. Do research and use your own words.

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5.1.3 **Component list**

List the components you will need for the circuit diagram.

LABEL	DESCRIPTION AND VALUE	QUANTITY

5.1.4 **Tools/Instrument list**

List the tools needed to complete the project.

DESCRIPTION	PURPOSE

5.2 Assessment of the Design and Make Phase: Part 1

NO.	FACET DESCRIPTION	Mark	Achieved mark
Circuit Diagram			
1.	The circuit diagram was drawn using ● EGD equipment (4) ● CAD/Any electronic design software (6)	6	
2.	The circuit diagram was drawn using correct symbols.	3	
3.	The circuit diagram has all labels, e.g. R1, C1, Tr1	3	
4.	The circuit diagram has all component values, e.g. 100 Ω, 220 µF	4	
5.	The circuit diagram has a name/title.	2	
6.	The circuit diagram has a frame and title block.	2	
	Circuit Diagram Subtotal:	**20**	
Component List			
7.	Labels correlate with circuit diagram.	2	
8.	Description and values correlate with circuit diagram.	2	
9.	Quantities are correct.	1	
	Component List Subtotal:	**5**	
Description of Operation			
10.	Basic function of the circuit is described correctly. The purpose/role/function of each component is described.	10	
11.	All subcircuits in the circuit diagram and component list are included in the description.	5	
12.	Purposes of subcircuits in the circuit diagram are described correctly.	5	
13.	Learner used own interpretation and did not copy from another source verbatim.	3	
14.	Sources are acknowledged.	2	
	Description of Operation Subtotal:	**25**	
Tools/Instrument List			
15.	The tools/instrument list has been completed.	4	
16.	All the tools/instruments listed have a purpose for being used.	1	
	Tools/Instrument List Subtotal:	**5**	

NO.	FACET DESCRIPTION	Mark	Achieved mark
Circuit Board Manufacturing			
17.	PCB layout designed with the use of computer software (4 marks)	4	
	PCB layout designed with the use of etching pens / Veroboard layout designed on paper (3 marks)		
18.	Transfer of the PCB design onto the blank board is correct. Not over-exposed or under-exposed.	5	
19.	Circuit board is etched neatly according to the PCB design.	10	
20.	The learner's name is etched onto the circuit design.	4	
21.	All burrs have been removed.	2	
22.	Axial and radial components are placed neatly and flush with the board.	5	
23.	Component orientation is aligned between similar components (e.g. the gold band of all resistors are placed on the same side).	2	
24.	Soldered components – leads are cut off, flush and neat on the solder side.	5	
25.	More than 60% of the solder joints are shiny (not dry joints).	5	
26.	Wire insulation is stripped to the correct length (no extra copper showing).	3	
27.	Wiring is long enough to allow for dismantling and inspection.	2	
28.	Wiring is wrapped neatly.	2	
29.	A power switch is included and fitted to the enclosure.	2	
30.	A fuse/protection is included and fitted correctly where applicable.	2	
31.	Wiring entering/exiting the enclosure is provided with a grommet/applicable fittings/sockets where applicable.	2	
32.	Batteries/Transformer is mounted using a battery housing/ mounting bracket and battery clip (NO double-sided tape).	2	
33.	The project has a pilot light/LED installed in the enclosure showing when the circuit is operational. LED is mounted with a grommet or applicable fitting. (Switch is on – must go out when fuse is blown.)	2	
34.	The project is fully operational and commissioned/installed in the enclosure.	6	
	Circuit Board Manufacturing Subtotal:	**65**	
	Circuit Diagram Subtotal:	**20**	
	Component List Subtotal:	**5**	
	Description of Operation Subtotal:	**25**	
	Tools/Instrument List Subtotal:	**5**	
	Circuit Board Manufacturing Subtotal:	**65**	

TOTAL (PART 1 = 120 marks)	

NOTE: If pre-etched and pre-manufactured PCB's are used, learners will not be able to receive any marks for facets 17-20.
In projects where facets are not applicable, the projects should be marked, and the totals adjusted accordingly.

5.3 Design and Make: Part 2

5.3.1 Enclosure design

- Design an enclosure for your project.
- NO FREEHAND DRAWINGS.
- Draw using EGD equipment **OR** use a CAD program.
- Draw in first-angle orthographic projection.
- Add your drawings after this page.
- Include the placement of ALL components/meters and holes in your drawing.
- Use colour to enhance your drawing.

5.3.2 Manufacture the enclosure neatly according to your design.

You may use pre-cut panels from metal, wood and/or Perspex/Plexiglas.
You must, however, construct/assemble these parts.
Injection-moulded enclosures are also acceptable. It is important that your enclosure and the placement of the parts align with your design.

5.3.3 Choose a name for your device.

Write down the name of the device below.

_____

5.3.4 Design a unique logo for your device, as well as a specification plate and attach it after this page.

Logo design	Specification plate design

5.4 Assessment of the Design and Make Phase: Part 2

NO.	FACET DESCRIPTION	Mark	Achieved mark
Enclosure Design			
1.	Enclosure design is included in first-angle orthographic projection.	2	
2.	Drawn design includes a title box and page border.	1	
3.	Isometric drawing included additionally.	2	
4.	Dimensions are included.	2	
5.	The name of the device is written in the PAT document.	1	
6.	The logo design and specification plate design are in the PAT document.	2	
	Enclosure Design Subtotal:	**10**	
Enclosure Manufacturing			
7.	Enclosure matches the design. Dimensions and placement correlate.	1	
8.	Name of the device is attached on the enclosure.	1	
9.	The logo design is attached on the enclosure.	2	
10.	The logo design on the enclosure is durable and not merely a paper pasted on the enclosure (painted/used decoupage/screen printed/sublimation printed).	2	
11.	The enclosure is manufactured from scratch/pre-cut parts. Perfectly manufactured square, neat and sturdy enclosure (5) Injection-moulded/pre-manufactured enclosures minimum alterations (3) Enclosures may include sheet metal, Perspex, Plexiglas, wood, glass and other raw materials, injection-moulded plastic boxes. Enclosures may NOT include cardboard, paper, margarine containers.	5	
12.	Holes/Cut-outs in the enclosure are made with the appropriate tools and match the design.	3	
13.	Specification plate with the learner's name, operating voltage, fuse rating and additional information on the project.	2	
14.	Enclosure is neatly prepared, painted and aesthetically pleasing.	2	
15.	The circuit board is mounted using appropriate methods inside the enclosure. (NO double-sided tape, Prestik, glue, chewing gum, masking tape, etc.)	2	
	Enclosure Manufacturing Subtotal:	**20**	

TOTAL (PART 2 = 30 marks)	

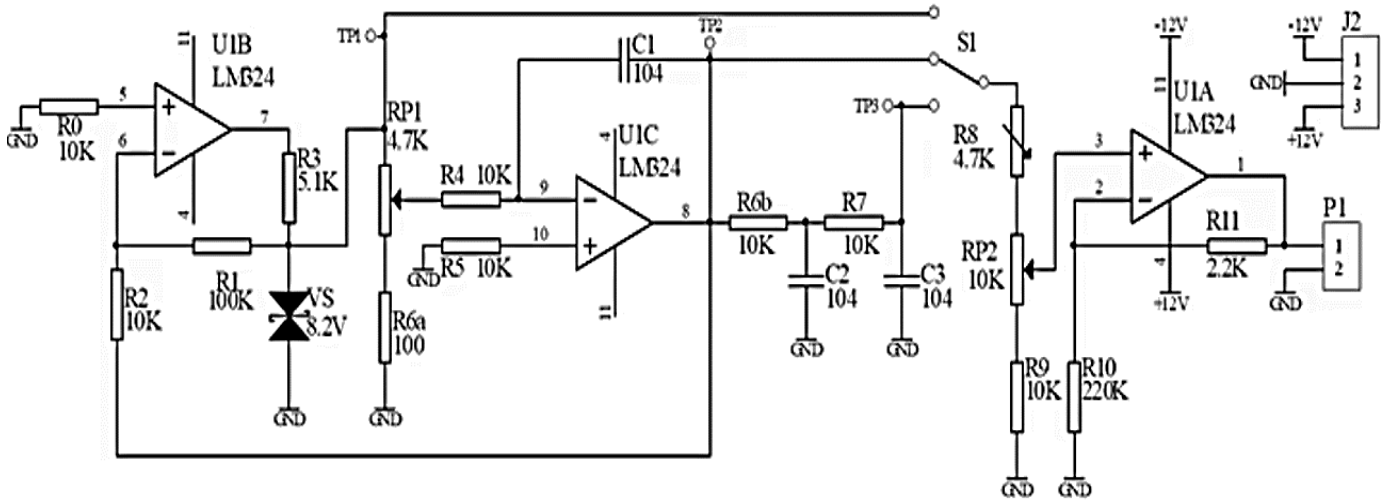
6. PROJECTS

6.1 Practical Project: Function generator

In the circuit diagram, U1A, U1B and U1C are three independent operational amplifiers inside an LM324 IC. The circuit composed by U1B is a comparator; the circuit composed by U1C, C1 and related circuits are an integrating circuit; the circuit composed by R6b, C2 and R7, C3 is a filter, which is used to filter out high harmonics and convert triangular waves into nearly triangular waves. The circuit consisting of R6b, C2, R7 and C3 is a filter for filtering out high harmonics and converting triangular waves to approximate sine waves. Rp2 is used to adjust the output amplitude and R8 and R9 are used to limit the maximum and minimum output signal amplitude.

The output of U1B (pin 7) feeds the output signal through R2,R1 to the input (pin 6), forming a positive feedback circuit.

The output signal from the output of U1C (pin 8) is also fed to the input of U1B (pin 6) via R2 to control the working state of U1B. The circuit consisting of U1C, C1 and the associated resistor is an integral circuit. The output of U1C (pin 8) outputs a triangular wave signal and adjusting RP1 can influence the charging and discharging time of this integral circuit, thus changing the frequency of the triangular wave. A high-pass filter consisting of R6b, C2, R7 and C3 is connected to the output of U1C (pin 8) to filter out the high frequency harmonics from the triangle wave and convert the triangle wave into an approximate sine wave.



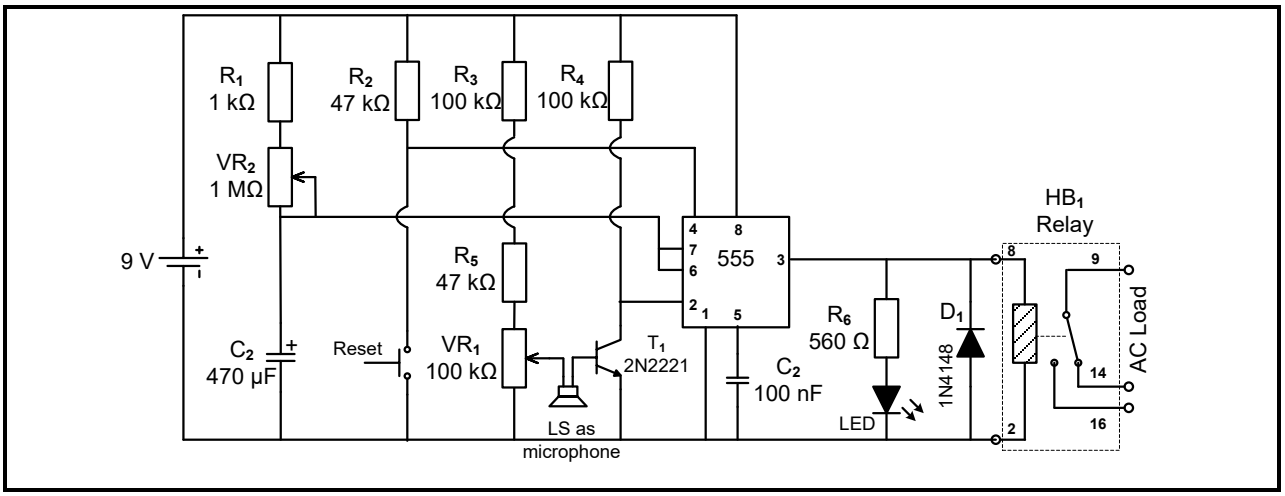
NOTE: All circuits MUST include an ON/OFF switch with an ON indicator and fuse protection.

6.2 Practical Project: Sound activated switch

This sound operated switch works with the popular 555 IC as a low current switching device that drives a relay as the AC switching device. The value at which VR2 is set, will determine the timing period. The triggering mechanism is a loudspeaker that is used as a microphone and is connected between the slider of VR1 and the base of transistor T1. If there is a loud noise or clap of hands close to the speaker, a small current generated by the speaker will flow through the transistor and if VR1 is set correctly, it will trigger the 555 IC. The value of VR1 is critical. First, turn it to its minimum. Then, while making a loud noise, very slowly adjust the potentiometer until the relay pulls on. Turn VR1 a shade, and it should be ready to fire when a load sound is made. If it is too sensitive, carefully adjust VR1 back a fraction more.

When there is a load noise or clap, the speaker will pick up the sound and generate a voltage, which is added to the voltage already on the slider of VR1. The sum of these two voltages will be sufficient to cause a small current to flow through T1, which, if VR1 is set fine enough, will pull the potential on the collector low enough to trigger the 555 IC. The timing period will be set by VR2 and C1. If the noise is not loud enough, insufficient voltage will be generated by the speaker (which is acting as a microphone), and the 33% threshold of pin 2 will not be reached and the 555 IC will not be triggered.

If it proves too difficult to set VR1, remove the wire connecting the emitter of T1 to 0 V and connect a 2k2 Ω resistor between the emitter and 0 V.



SOUND ACTIVATED SWITCH WITH 555 IC AND RELAY

Component list

D1	1N4148	VR1	100 kΩ
C1	470 µF	VR2	1 MΩ
C2	100 nF	R1	1 kΩ
LS	Loudspeaker/Microphone	R2&R5	47 kΩ
T1	2N2221 NPN Transistor	R3&R4	100 kΩ
Varistor	MOV RDN240/20	R6	560 Ω
IC1	555 IC	S1	SPST switch
LED	Red LED 5 mm	Fuse	250 mA
Supply 9 V DC with battery holder			
Relay – 9 V DC coil, SPDT 10 A/250 V			

NOTE: All circuits MUST include an ON/OFF switch with an ON indicator and fuse protection.

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7. CONCLUSION

On completion of the practical assessment task, learners should be able to demonstrate their understanding of the industry, enhance their knowledge, skills, values and reasoning abilities as well as establish connections to life outside the classroom and address real-world challenges. The PAT furthermore develops learners' life skills and provides opportunities for learners to engage in their own learning.

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