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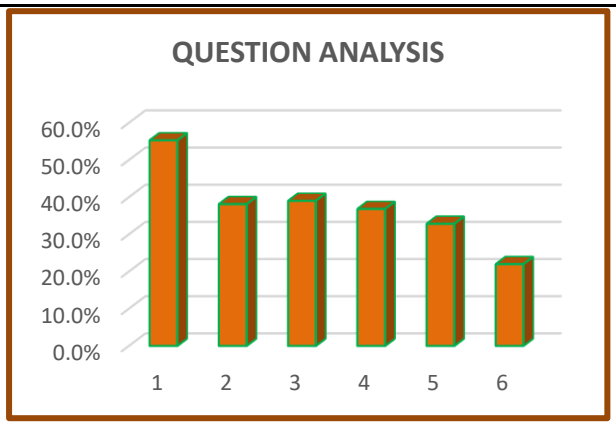
QUALITATIVE ANALYSIS OF LEARNER RESPONSES
AND
EVALUATION OF THE QUESTION PAPERS (PER PAPER)
NATIONAL SENIOR CERTIFICATE 2025
WESTERN CAPE EDUCATION DEPARTMENT

SUBJECT	**ELECTRICAL TECHNOLOGY (DIGITAL SYSTEMS)**		
QUESTION PAPER	**1**	**2**	**3**
DURATION OF PAPER	**3 HOURS**		
INTERNAL MODERATOR	**WEN JOSEPH**		
CHIEF MARKER	**G CONRADIE**		
DATES OF MARKING	**FROM: 29 NOVEMBER 2025**	**TO: 10 DECEMBER 2025**	
HEAD OF EXAMINATION	**MS LM BREDENKAMP**		

REPORT 2: QUALITATIVE ANALYSIS OF LEARNER RESPONSES

SECTION 1: ***(GENERAL OVERVIEW OF LEARNER PERFORMANCE IN THE QUESTION PAPER AS A WHOLE)***

QUESTION NUMBER	1	2	3	4	5	6	
TOTAL	15	10	50	20	55	50	
SUM	224	103	527	199	488	297	200
AVERAGE %	55.3%	38.1%	39.0%	36.9%	32.9%	22.0%	1838
AVERAGE MARK	8.3	3.8	19.5	7.4	18.1	11.0	34.0%
RANGE	12	8	36	15	46	39	68.1
RANGE %	80.0%	80.0%	72.0%	75.0%	83.6%	78.0%	139
MEDIAN	8	4	17	7	17	8	69.5%
MEDIAN %	53.3%	40.0%	34.0%	35.0%	30.9%	16.0%	63
STANDARD DEVIATION	3.4	1.9	10.3	4.4	13.2	10.8	31.5%



CODE DISTRIBUTION		
Code	**Range**	**Number**
7	≥90%	0
7	80% - 89%	0
6	70% - 79%	3
5	60% - 69%	1
4	50% - 59%	1
3	40% - 49%	2
2	30% - 39%	8
1	20% - 29%	5
1	0% - 19%	7
	TOTAL	**27**

Overall learner performance in the Digital Electronics paper was **below the expected Grade 12 standard**, with the majority of candidates achieving low to moderate marks and only a small number performing well across all sections of the paper. The uploaded recording sheet shows clear patterns of **content gaps**, **incomplete responses**, and **difficulty with higher-order questions**, which collectively indicate that the cohort was not fully prepared for the demands of the examination.

Learners generally performed **better in low-order recall questions**, such as definitions, basic logic identification, and straightforward digital concepts (e.g., safety questions and basic device functions). These items allowed most candidates to earn accessible marks.

However, performance declined sharply in **middle- and higher-order questions** requiring application, interpretation, and multi-step reasoning. In particular:

- **Question 6 (Microcontrollers and digital communication)** shows the **lowest marks across the cohort**, with many learners scoring between **0 and 2 marks**, and several leaving large sections blank.
- **Sequential logic**, including flip-flop behaviour, counters, and register operations, also shows **weak performance**, with many learners unable to complete logic sequences or predict circuit behaviour.
- Questions involving **timing diagrams, waveform interpretation, and op-amp switching circuits** were poorly answered, indicating limited conceptual understanding and insufficient practice with visual or multi-step problem-solving tasks.

The overall distribution of marks reflects a **downward shift** compared to what is typically expected:

- Few learners achieved marks above 60%,
- A large concentration of learners fall within the **30–49% range**, and
- Several candidates performed below 30%, signalling significant conceptual gaps.

The pattern of responses—including blank sections, partial attempts, and incorrect reasoning—strongly suggests that learners entered the examination with **gaps in curriculum coverage**, especially in microcontroller content that should have been taught in Term 3. This incomplete preparation directly contributed to the overall weaker performance.

In summary:

The cohort demonstrated basic recall skills but struggled substantially with application and higher-order reasoning. Performance across the paper shows that learners were **not sufficiently prepared**, particularly in the latter sections that carry significant weight, resulting in generally low totals and weaker outcomes compared to expected Grade 12 standards.

SECTION 2: *COMMENT ON CANDIDATES' PERFORMANCE IN INDIVIDUAL QUESTIONS*

(It is expected that a comment will be provided for each question)

QUESTION 1
(a) General comment on the performance of learners in the specific question. Was the question well answered or poorly answered?
Question 1 was **moderately answered**. Most items in this section required **basic recall and straightforward understanding**, and candidates generally performed better here than in later questions. However, several learners still selected incorrect options, indicating that foundational knowledge was not secure across the entire cohort.
(b) Why was the question answered poorly? Also provide specific examples, indicate common errors committed by learners in this question, and any misconceptions.
Learners' errors in Question 1 were **less about calculation or deep content gaps** and more about ineffective **MCQ-answering technique**. Evidence from the paper and memo shows the following: **Specific issues observed:** • **Not reading the full stem** of the question before selecting an answer, leading to incorrect choices on terms such as *reference voltage*, *trigger*, or *input condition*, which recur throughout the paper. • **Failure to eliminate obviously incorrect options**—several distractors in the paper are clearly wrong when compared with the definitions in the marking guideline, yet many learners still selected them. • **Misinterpretation of logic symbols or device functions**, despite these being used repeatedly in later diagrams (adders, seven-segment display, flip-flops). • **Choosing familiar-sounding terms rather than correct technical definitions**, e.g., selecting an option with "supply voltage" instead of the correct "comparison level" when describing reference voltage. **Typical misconceptions reflected in MCQ choices:**

- Believing trigger or threshold levels operate the same for all multivibrator circuits, despite the specific definitions used in the paper's timer questions.
- Confusing the function of op-amp inputs (inverting vs non-inverting) when asked to define related terms.
- Thinking propagation delay refers to wiring length instead of flip-flop/counter timing, as clarified in the memo.

These patterns show that learners **did not approach MCQs analytically**, and instead often guessed or relied on surface familiarity.

(c) Provide suggestions for improvement in relation to Teaching and Learning.

To improve performance in MCQs specifically, teaching should support both **content mastery** and **MCQ methodology**:

1. Teach explicit MCQ strategies:

- Read the entire question stem before looking at the options.
- Highlight keywords such as *trigger*, *threshold*, *reference*, *input condition*.
- Use elimination: cross out options that contradict basic Digital Electronics principles.
- Compare remaining options to the definitions used in class and reflected in the memo.

2. Practise MCQ items that match the style of the paper:

- Use the same circuit formats, symbols, and definitions that appear in the exam.
- Provide past Q1 items for revision so learners become familiar with distractor patterns.

3. Link MCQs to diagrams used later in the paper:

- Show learners how definitions in Q1 directly relate to content in Q3 (timers), Q4 (op-amps), and Q5 (logic devices).
- Reinforce understanding through conceptual, not memorised, learning.

4. Encourage learners to justify their MCQ choices during practice:

- Require short verbal or written explanations to build conceptual clarity and prevent guessing.

(d) Describe any other specific observations relating to responses of learners and comments that are useful to teachers, subject advisors, teacher development etc.

 Incorrect MCQ selections indicate **shallow understanding of core terms**, which later undermined performance in Section B, where those same terms determine circuit behaviour.

 Teachers may benefit from support in developing **diagnostic MCQ activities** that reveal misconceptions early in the year.

 Many distractor choices made by learners suggest they were **not looking for technical precision**, which is essential in Digital Electronics; training learners to read MCQs critically would improve performance across the paper.

 Advisors should encourage schools to integrate **regular low-stakes MCQ assessments** to ensure learners are comfortable with the exam format.

QUESTION 2

(a) General comment on the performance of learners in the specific question. Was the question well answered or poorly answered?

Question 2 carried **10 marks** in total and assessed OHSA knowledge through short, direct theory questions. Despite the relatively low cognitive demand, the question was **poorly answered** by many learners.

Most candidates earned only **2–4 marks out of 10**, while very few achieved full marks. This indicates that even basic safety terminology was not well understood or correctly expressed.

(b) Why was the question answered poorly? Also provide specific examples, indicate common errors committed by learners in this question, and any misconceptions.

Learners struggled to provide the **formal OHSA definitions** required to earn the full mark allocation per item.

Examples of mark-related errors:

- Many responses were **too short** to earn the full **2 marks** allocated for each definition.
- Some learners wrote **generic descriptions** that earned **0 marks** because they did not match the memo wording.
- Where 2 marks were allocated for a two-part definition (e.g., identifying the hazard *and* describing its consequence), learners often only wrote one component, earning **1 mark instead of 2**.

Common misconceptions tied to mark loss:

- **Dangerous practice** was described as "doing something unsafe," without specifying how it *creates a risk*, resulting in **0 marks**.
- **Critical incident** was defined vaguely as "a big accident," which did not meet the memo requirement for **2-mark completeness**.
- **Unsafe condition** was confused with "unsafe behaviour," losing the full **2 marks** for that item.
- **Machinery** was incorrectly described as "any electrical equipment," which did not meet the definition in the memo.

In short, learners repeatedly provided answers that lacked the detail needed to earn the allocated marks.

(c) Provide suggestions for improvement in relation to Teaching and Learning.

1. Teach the structure of a full-mark definition

Where questions allocate **2 marks**, learners need to be taught that acceptable answers usually contain **two required components**. Practice should involve identifying these components from past memos.

2. Use memo-aligned wording

Since the memo awards marks for *specific elements*, teachers should emphasise precise vocabulary, not loose descriptions.

3. Provide mark-based practice tasks

Have learners answer OHS questions and then mark them using the memo's criteria (e.g., 0/1/2 marks), helping them understand how wording affects marks.

4. Reinforce differences between similarly marked terms

Tasks that compare *dangerous practice*, *critical incident*, and *unsafe condition* help learners avoid losing marks through confusion.

(d) Describe any other specific observations relating to responses of learners and comments that are useful to teachers, subject advisors, teacher development etc.

- Many learners earned **less than half of the 10 marks available**, indicating that OHSA content may not have been emphasised in teaching, even though it offers accessible marks.
- Teachers may need support in delivering **exam-style definitions**, as inconsistent classroom terminology can lead to mark loss.
- For many learners, OHS could have been a "safe" scoring section, but poor preparation meant marks were lost unnecessarily.
- Improving OHS instruction would raise overall totals, since these **10 marks** are among the easiest to secure in the paper.

QUESTION 3

(a) General comment on the performance of learners in the specific question. Was the question well answered or poorly answered?

Question 3 was **poorly answered across the cohort**, despite its large contribution of **50 marks** to the paper. Most learners achieved **very low to mid-range scores**, with many falling below 20/50. Only a small number of candidates scored above 30 marks.

Although Question 3 included a combination of definition/explanation items, diagram interpretation, and short application questions, performance indicates that learners **lacked both conceptual understanding and the ability to interpret switching-circuit behaviour**.

(b) Why was the question answered poorly? Also provide specific examples, indicate common errors committed by learners in this question, and any misconceptions.

Learners struggled throughout Question 3 because the required concepts—particularly switching thresholds, multivibrator behaviour, op-amp operation, and waveform reasoning—were not well understood. The large mark allocation magnified these gaps.

Below is a breakdown tied to the kinds of items asked and the patterns seen in the marks:

1. Definitions and explanations (worth multiple 2–4 mark items)

Many learners wrote **vague or incomplete explanations**, earning **0–1 mark** instead of the full allocation.

Typical errors included:

- Describing a *reference voltage* incorrectly as the supply voltage.

- Giving generic statements such as "the output changes" without referring to thresholds or input conditions.
- Mixing up bistable and monostable functions.

These errors caused large cumulative mark losses because Question 3 contained multiple short-explanation items.

2. Circuit behaviour and operational reasoning (several 4–6 mark items)

Learners struggled to explain:

- what happens when threshold components (R1, R2) are bypassed,
- how a Schmitt trigger switches at the upper threshold,
- the effect of input rising/falling edges on output waveform.

Misconceptions:

- Believing comparators switch continuously instead of at threshold crossings,
- Confusing a bistable's stable states with monostable timing,
- Thinking changes occur "automatically" rather than in response to defined input levels.

Learners tended to give **descriptive but technically incorrect** answers, earning partial or no marks.

3. Waveform interpretation (several items worth 4–8 marks)

This was one of the weakest areas.

Common issues:

- Learners could not relate input conditions to output waveforms.
- Many assumed the output matches the input shape—incorrect for comparators and differentiators.
- Few referenced or applied threshold levels (1/3 VCC and 2/3 VCC), even though these control switching.

This section contributed heavily to low totals because waveform items carry large mark allocations.

4. Differentiator behaviour (4–6 mark items)

A major misconception was treating the differentiator as a normal amplifier.

Frequent incorrect answers:

- "The output is the same shape as the input."
- "The output increases the voltage of the input."
- No mention of *rate of change*, *spikes*, or *edge emphasis*, which the memo required.

This resulted in whole-mark losses on an item many learners attempted but answered incorrect.

(c) Provide suggestions for improvement in relation to Teaching and Learning.

1. Use simulations and visual tools

Comparator, Schmitt trigger, bistable, and differentiator behaviour should be demonstrated visually. Learners who only encounter theory struggle to link circuit behaviour to waveforms.

2. Teach structured explanation techniques

For a 2–4 mark explanation, learners should be taught to:

- reference the specific input condition (threshold, trigger, rising/falling edge),
- explain the resulting output behaviour step by step,
- avoid vague statements ("the output changes").

3. Focus more on waveform reasoning skills

Waveform prediction is a consistent weakness.

Regular practice should include:

- drawing outputs from inputs,
- justifying waveform transitions,
- relating circuit elements to timing changes.

4. Reinforce foundational switching concepts

Clear, repeated teaching is needed on:

- threshold levels (1/3 and 2/3 VCC),
- stable vs unstable states,
- how op-amp comparators behave.

(d) Describe any other specific observations relating to responses of learners and comments that are useful to teachers, subject advisors, teacher development etc.

- Learners' responses show **rote learning rather than conceptual understanding**.
- Weakness in Question 3 directly affected performance in later questions that depend on the same principles (e.g., op-amp behaviour in Q4).
- Teachers may require **professional development** on teaching waveform interpretation, switching circuits, and op-amp behaviour using real examples.
- The depth required in Question 3 (50 marks) highlights that this section must be taught systematically across the year, not in isolation.

QUESTION 4

(a) General comment on the performance of learners in the specific question. Was the question well answered or poorly answered?

Learner performance in Question 4 was **poor**, with most candidates achieving **4–9 out of 20**, and only a small number reaching double-digit scores.

Although the question carried fewer marks than Q3, it still required **clear conceptual understanding**, and the cohort struggled across almost all parts of the question. This section contributed noticeably to low overall totals.

(b) Why was the question answered poorly? Also provide specific examples, indicate common errors committed by learners in this question, and any misconceptions.

Learners struggled to:

- describe behaviour using correct technical vocabulary,
- differentiate between input conditions and resulting output,

- express answers concisely but completely.

These sub-questions typically required **2-mark explanations**, yet many learners provided only one idea, earning **1 mark** or none.

(c) Provide suggestions for improvement in relation to Teaching and Learning.

1. Strengthen foundational understanding of op-amp stages

Teachers should use block diagrams and simulations to show how each stage contributes to overall operation.

2. Emphasise explanation-based responses

Because several 2-mark items in this question required *cause-and-effect* reasoning, learners should practise:

- referring to the specific input condition,
- describing the resulting output behaviour,
- explaining *why* the behaviour occurs.

3. Provide regular practice with summing and differentiator circuits

Learners need repeated exposure to interpreting:

- inverting summing amplifiers,
- differentiator action,
- effects of waveform edges.

4. Use memo-aligned teaching terminology

The marking guideline requires specific phrases (e.g., "rate of change," "differential input stage," "voltage gain stage"). Using these consistently in class reduces mark loss.

(d) Describe any other specific observations relating to responses of learners and comments that are useful to teachers, subject advisors, teacher development etc.

- Many learners attempted Question 4 but demonstrated **rote familiarity** rather than understanding, indicating that op-amp applications may not have been taught with sufficient depth.
- Responses show a lack of exposure to **visual and functional interpretation** of op-amp circuits — suggesting a need for more practical demonstrations or simulations.
- Learners' difficulties in this section also affected performance in later questions involving analog-to-digital behaviour or switching logic, showing the foundational importance of Question 4 content.
- Teacher development could focus on strengthening strategies to teach **conceptual op-amp behaviour**, not just circuit formulas.

QUESTION 5

(a) General comment on the performance of learners in the specific question. Was the question well answered or poorly answered?

Question 5 was **poorly answered overall**, despite covering core Digital Electronics content that

Grade 12 learners are expected to master.

Most candidates scored **between 10–25 out of 55**, with very few exceeding 30. Several learners scored below 10, indicating substantial gaps in sequential reasoning and digital circuit interpretation.

Because this question carries a very large mark weighting, poor performance here had a strong negative influence on total scores.

(b) Why was the question answered poorly? Also provide specific examples, indicate common errors committed by learners in this question, and any misconceptions.

Learners struggled throughout Question 5 due to weak understanding of sequential logic and limited ability to interpret or apply state-based behaviour. Errors were consistent across the following sub-sections:

1. Seven-segment decoding (±8 marks)

Observed errors:

- Incorrect segment labels or missing segments.
- Confusion between common-anode and common-cathode outputs.
- Incorrect activation patterns for the required number.

Mark impact:

Typical scripts earned **2–4/8**, rather than full marks.

2. Half-adder / full-adder logic (±10 marks)

Common errors:

- Incorrect truth tables, especially for the carry output.
- Misidentifying the sum output as OR rather than XOR.
- Writing Boolean expressions not matching the memo.

Misconception:

Many learners believe the sum output is OR logic, which led to systematic mark loss.

Mark impact:

Several candidates earned **2–5/10**, with very few achieving the full allocation.

3. JK flip-flop operation (±12 marks)

This was one of the weakest areas of Question 5.

Typical errors:

- Not applying toggle behaviour when **J = K = 1**.
- No reference to **clock edges**, despite the memo requiring this.
- Writing state sequences unrelated to the actual transitions of a JK device.
- Misinterpreting the initial conditions.

Mark impact:

Many learners scored **0–3/12** because incorrect sequences receive no partial credit when they contradict device behaviour.

4. Asynchronous counter sequence (±14–16 marks)

This section produced the lowest scores.

Common errors:

- Assuming all flip-flops change state simultaneously.
- Ignoring propagation delay, even though ripple timing determines the count sequence.
- Writing sequences in reverse or skipping states.
- Not identifying which flip-flop acts as the "clock" for the next stage.

Misconceptions:

- Belief that each flip-flop toggles on every external clock pulse.
- Thinking that counters behave the same as shift registers.

Mark impact:

Multiple learners received **0–2 marks out of 16**.

This sub-section alone explains much of the downward shift in overall performance.

5. Registers and storage behaviour (remainder of marks)

Common errors:

- Incorrect direction of shifting (left vs right).
- Misunderstanding when data moves (clock-edge dependent).
- Assuming that all stored bits update simultaneously.

Mark impact:

Most candidates earned **1–3 marks**, instead of the full allocation.

(c) Provide suggestions for improvement in relation to Teaching and Learning.

1. Teach sequential logic using step-by-step state reasoning

Learners must be trained to evaluate, at each clock pulse:

- input conditions (J, K, D, etc.),
- clock edge,
- previous state,
- resulting next state.

This methodology must be explicitly taught and practised.

2. Provide extensive practice with truth tables and timing diagrams

Question 5 depends heavily on learners being fluent with:

- JK truth tables,
- counter ripple timing,
- register shifting behaviour,
- seven-segment logic.

Regular practice using exam-style questions is essential.

3. Use digital simulations for demonstration

Tools such as Logisim, Yenka, Multisim, or Tinkercad Circuits help learners visualise:

- sequential state changes,
- propagation delay in asynchronous counters,
- flip-flop toggling,
- seven-segment decoding.

Concepts in Question 5 become far more accessible when observed in motion.

4. Reinforce correct terminology aligned with the memo

Learners consistently lose marks for:

- incorrect naming of adders,
- incorrect flip-flop states,
- misuse of terms like *toggle*, *propagation delay*, *carry*, *register*.

Teachers should model and enforce memo-aligned definitions and explanations.

(d) Describe any other specific observations relating to responses of learners and comments that are useful to teachers, subject advisors, teacher development etc.

 Learners' answers indicate **rote memorisation without conceptual understanding**, especially in counter and flip-flop questions.

 Poor sequential-logic reasoning suggests that this topic may not have been sufficiently practised throughout the year.

 The very low marks on the counter section show that learners require **explicit instruction on ripple delay**, a concept that is often only briefly covered.

 Teacher development should focus on **teaching state-based logic using diagrams and interactive tools**, not purely theoretical notes.

 Because Question 5 carries **55 marks**, ensuring strong teaching here would significantly raise overall examination performance.

QUESTION 6

(a) General comment on the performance of learners in the specific question. Was the question well answered or poorly answered?

Learner performance in Question 6 was **very poor**, even though it carried the **highest mark allocation in the entire written paper (50/200 = 25%)**.

Based on the mark sheet, most candidates scored only **5–15 out of 50**, with some scoring lower than 5. Very few achieved above 20.

This indicates widespread lack of preparation in microcontroller content.

(b) Why was the question answered poorly? Also provide specific examples, indicate common errors committed by learners in this question, and any misconceptions.

6.1 – Define a microcontroller (3 marks)

Most learners provided vague answers such as "a small computer" without mentioning the

required components (CPU, memory, I/O).

Common marks: 0–1/3.

6.2 – TRIS register & labeling (5 marks)

(6.2.1: 1 mark, 6.2.2: 4 marks)

Learners struggled to describe:

- **What TRIS does (1=input, 0=output),**
- **Why direction setting is required**,
- **Bit-to-pin mapping**.

Many gave answers that earned **0–1/5**.

6.3 – Synchronous communication (11 marks)

Breakdown:

- 6.3.1 (Label A & B): 2 marks
- 6.3.2 (How data is transferred): 3 marks
- 6.3.3 (Accuracy ensured): 4 marks
- 6.3.4 (Two advantages): 2 marks

This entire section was poorly answered because:

- Learners could not explain **clock-based synchronisation**.
- They did not reference *shift registers*, *timing edges*, or *data sampling*.
- Many confused synchronous with serial asynchronous (UART).

Most learners scored **0–3/11**.

6.4 – UART + naming another peripheral (4 marks)

(6.4.1 = 3 marks, 6.4.2 = 1 mark)

Common errors:

- Incorrectly describing UART as "parallel communication."
- Not mentioning *buffering, start/stop bits, or serial frame structure*.

Typical scores: **1–2/4.**

6.5 – Half duplex vs full duplex (2 marks)

Learners often reversed the definitions or gave unclear descriptions.

Many achieved **0/2**.

6.6 – SPI bus (8 marks)

Breakdown:

- 6.6.1 Label A & B: 2 marks
- 6.6.2 Meaning of MOSI: 1 mark
- 6.6.3 Advantages: 3 marks
- 6.6.4 Function: 2 marks

Learners commonly:

- Mixed up *MOSI* and *MISO*,
- Failed to list three correct advantages,
- Did not describe SPI as a **full-duplex, clock-driven synchronous communication system**.

Most scripts scored **1–3/8**.

6.7 – Definitions: Looping, Condition, Instruction cycle (7 marks)

Breakdown:

- Looping: 2 marks
- Condition: 2 marks
- Instruction cycle: 3 marks

Errors included:

- Vague statements such as "repeat the program,"
- No explanation of *fetch–decode–execute*.

Typical scores: **1–3/7**.

6.8 – Flowchart completion (10 marks)

This is the single biggest section and was the **worst performed**.

Reasons:

- Learners could not apply **counting logic** (500 travellers limit).
- Missing or incorrect loop structure.
- Incorrect sequencing of *sensor triggers* and light control.
- Many answers left blank.

Most learners scored **0–2/10**.

(c) Provide suggestions for improvement in relation to Teaching and Learning.

- **Teach TRIS, PORT, and bit-direction control explicitly** using table exercises.
- **Use microcontroller simulators** (PICAXE Editor, Proteus, Tinkercad) to demonstrate register behaviour.
- **Reinforce synchronous vs asynchronous communication** with diagrams and timing examples.
- **Practice interpreting and completing flowcharts**, especially with counters and conditions.
- **Teach communication peripherals** (UART, SPI, I²C) using block diagrams and real examples.

(d) Describe any other specific observations relating to responses of learners and comments that are useful to teachers, subject advisors, teacher development etc.

- The extremely low performance suggests **limited curriculum coverage** of microcontroller topics, possibly linked to **PAT project time interfering with Term 3 teaching**, as noted.
- This question depends heavily on logical reasoning, which was not demonstrated by the majority of learners.
- Because Q6 carries **50 marks**, lack of competence here severely depresses overall results.
- Teacher training should focus on **hands-on microcontroller instruction**, not theoretical summaries.