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EDUCATION

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NATIONAL SENIOR CERTIFICATE

GRADE 12

SEPTEMBER 2026

ELECTRICAL TECHNOLOGY: DIGITAL ELECTRONICS MARKING GUIDELINE

MARKS: 200

This marking guideline consists of 12 pages.

INSTRUCTIONS TO MARKERS

1. All calculations with multiple answers imply that any relevant, acceptable answer should be considered.
2. Calculations:
 - 2.1 All calculations must show the formulae.
 - 2.2 Substitution of values must be done correctly.
 - 2.3 All answers **MUST** contain the correct unit to be considered.
 - 2.4 Alternative methods must be considered, provided that the correct answer is obtained.
 - 2.5 Where an incorrect answer could be carried over to the next step, the first answer will be deemed incorrect. However, should the incorrect answer be carried over correctly, the marker has to re-calculate the values, using the incorrect answer from the first calculation. If correctly used, the candidate should receive the full marks for subsequent calculations.
 - 2.6 Markers should consider that learners' answers may deviate slightly from the marking guideline depending on how and where in the calculation rounding off was used.
3. This marking guideline is only a guide with model answers.
4. Alternative interpretations must be considered and marked on merit. However, this principle should be applied consistently throughout the marking session at ALL marking centers.

QUESTION 1: MULTIPLE-CHOICE QUESTIONS

- 1.1 A ✓
- 1.2 B ✓
- 1.3 C ✓
- 1.4 B ✓
- 1.5 C ✓
- 1.6 B ✓
- 1.7 B ✓
- 1.8 B ✓
- 1.9 A ✓
- 1.10 B ✓
- 1.11 D ✓
- 1.12 B ✓
- 1.13 B ✓
- 1.14 B ✓
- 1.15 A ✓

[15]**QUESTION 2: OCCUPATIONAL HEALTH AND SAFETY**

- 2.1
- Improper handling of hand tools. ✓
 - Misuse of electrical equipment. ✓
 - Chemical exposure (etching solutions).
 - Poor workshop housekeeping/clutter.
 - Inadequate personal protective equipment.
 - Faulty or damaged equipment.
- (Any TWO answers are correct) (2)
- 2.2
- 2.2.1 This is an unsafe condition ✓ because it is a physical hazard in the environment (not a worker's action). Poor lighting increases the risk of errors, eye strain, and accidents. ✓ (2)
- 2.2.2 This is an unsafe act ✓ because it is a deliberate or careless action by the worker ✓ that violates safety procedures. Untrained operators risk burns, inhalation of fumes, or damaging equipment. (2)
- 2.3
1. **Identification of hazards** ✓ – Conduct a walkthrough inspection to identify all potential hazards (electrical, chemical, mechanical, ergonomic).
 2. **Assessment of risk level** ✓ – Evaluate each hazard using descriptive categories (high, medium, low) based on likelihood and severity.
 3. **Vulnerability analysis** ✓ – Determine which personnel or equipment are most vulnerable to each hazard.
 4. **Implementation of control measures** ✓ – Devise counter-measures or mitigation strategies (engineering controls, administrative controls, PPE).
 5. **Documentation and review** ✓ – Record findings and schedule periodic reassessment.

(4)
[10]

QUESTION 3: SWITCHING CIRCUITS

3.1 3.1.1 Bistable multivibrator ✓

3.1.2 It has two stable output states (HIGH and LOW). ✓

It remains in a given state indefinitely until externally triggered. ✓

It does not oscillate freely without input. ✓

Two external inputs.

It requires SET and RESET inputs to change state.

Output state is determined by the last input applied.

It functions as a memory element or latch.

(Any three answers)

(3)

3.1.3 If R3 is removed, an excessively high current will flow through the LED ✓
when the output (Pin 3) is HIGH. This excessive current will cause the LED to burn out and potentially damage ✓ the 555 timer's output stage. (2)

3.1.4 The switch momentarily connects the common junction ✓ (pin 6/pin 2 connection point) to ground (0V).

Pin 2 (trigger input) is pulled below $\frac{1}{3}V_{CC}$ ✓ (which is approximately 2V for a 6V supply).

This triggers the internal comparator, ✓ causing the SR flip-flop to SET.

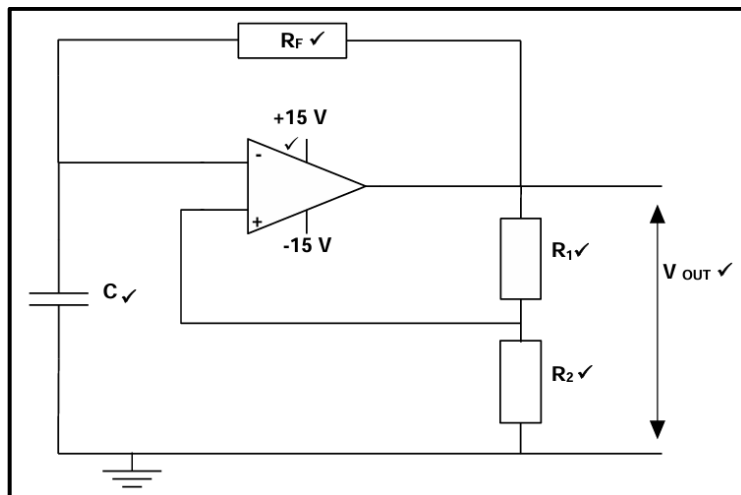
The output at Pin 3 immediately switches to HIGH (+6V), ✓ illuminating the LED.

The output remains HIGH ✓ until the RESET switch is pressed.

(5)

3.1.5 These resistors are known as 'pull-up' resistors. ✓ When both SET and RESET buttons are open, the pull-up resistors keep the voltage on the input high. ✓ (2)

3.2



(6)

3.3 Pulse generation/shaping ✓

Time delay circuits ✓

Missing pulse detector

Frequency divider

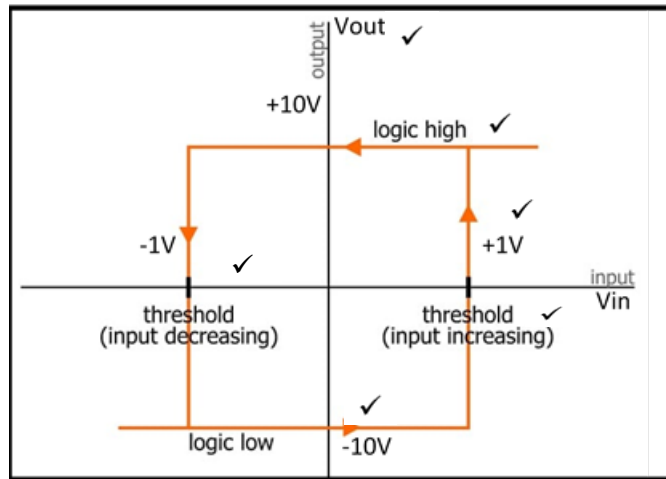
Debounce circuit for switches

One-shot timer

(Any TWO correct answers)

(2)

3.4



(6)

- 3.5 3.5.1 A summing amplifier ✓ combines multiple input signals into a single output signal whose magnitude is proportional to the sum of the input voltages. ✓ It performs signal addition in the analog domain, with the output typically inverted (180° phase shift). (2)

$$\begin{aligned}
 3.5.2 \quad V_{OUT} &= -R_F \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) \checkmark \\
 -8,0 &= -R_F \left(\frac{0,180}{10\,000} + \frac{0,220}{10\,000} + \frac{0,400}{10\,000} \right) \checkmark \\
 -8,0 &= -R_F (0,000018 + 0,000022 + 0,000040) \\
 -8,0 &= -R_F (0,00008) \\
 8,0 &= R_F \cdot 0,00008 \\
 R_F &= \frac{8,0}{0,00008} \\
 &= 10\,000\,000\,\Omega = 100\,k\Omega \checkmark
 \end{aligned}
 \quad (3)$$

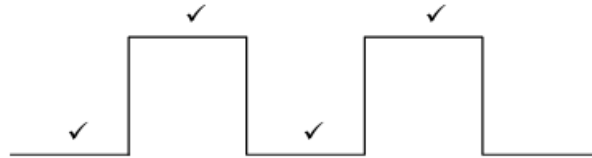
$$\begin{aligned}
 3.5.3 \quad A_V &= -\frac{R_F}{R_{in}} \checkmark \\
 &= -\frac{100\,000}{10\,000} \checkmark \\
 &= -10 \checkmark
 \end{aligned}
 \quad (3)$$

$$\begin{aligned}
 3.5.4 \quad V_{OUT} &= -R_F \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) \checkmark \\
 &= -100\,000 \left(\frac{0,180}{20\,000} + \frac{0,220}{10\,000} + \frac{0,400}{10\,000} \right) \checkmark \\
 &= -100\,000 (0,000009 + 0,000022 + 0,000040) \\
 &= -100\,000 (0,000071) \\
 V_{out} &= -7,1\,V \checkmark
 \end{aligned}
 \quad (3)$$

- 3.5.5 In this configuration, the input signals are fed into the inverting (-) terminal, while the non-inverting (+) terminal is connected to ground (0V). ✓ This design ensures that as the input voltage increases, the output voltage decreases, causing a polarity inversion or 180-degree phase shift. ✓ (2)

- 3.6 The less light shone on the LDR, the higher the resistance. ✓ If the LDR resistance increases, the voltage increases over the non-inverting input, ✓ switching the output of comparator high (1). ✓
 The more light shone on the LDR, the lower the resistance. ✓ If the LDR resistance decreases, the voltage will decrease over the non-inverting input, ✓ switching the output of comparator low (0). ✓ (6)

3.7



(4)
[50]

QUESTION 4: SEMICONDUCTOR DEVICES

- 4.1 Infinite input impedance (prevents loading of input source). ✓
 Zero output impedance (can deliver current without voltage drop). ✓
 Infinite voltage gain (amplifies any signal difference). ✓
 Infinite bandwidth (amplifies all frequencies equally). ✓
 Zero offset voltage (output is zero when inputs are equal).
 Infinite slew rate (output changes instantaneously).
 Perfect frequency response (flat gain across all frequencies).
 High common-mode rejection ratio (rejects unwanted common signals).
 (Any FOUR answers) (4)

4.2 4.2.1 $A_V = 1 + \frac{R_F}{R_{IN}}$ ✓
 $A_V = 1 + \frac{75\,000}{15\,000}$ ✓
 $A_V = 1 + 5 = 6$ ✓ (3)

4.2.2 $V_{OUT} = V_{IN} \times A_V$ ✓
 $V_{OUT} = 2,5 \times 6$ ✓
 $V_{OUT} = 15\,V$ ✓ (3)

- 4.2.3 If the feedback resistance (R_f) is decreased:

The voltage gain decreases (since $A_V = 1 + \frac{R_F}{R_{IN}}$). ✓
 The output voltage becomes smaller for the same input voltage. ✓
 The circuit becomes less sensitive to input signals.
 The amplifier provides less amplification.
 (Any TWO answers) (2)

- 4.3 4.3.1 The signal will be 10 times greater than the input signal/the output will be 1V ✓ and the output signal will be 180° out of phase with the input signal. ✓ (2)
- 4.3.2 The signal will be 11 times greater than the input signal / the output will be 1,1 V ✓ and the output signal will be in phase with the input signal. ✓ (2)
- 4.4 4.4.1 Serves as the input to the upper comparator inside the 555 timer. ✓
Compares the voltage at this pin to $\frac{2}{3}V_{cc}$ reference voltage. ✓
When the threshold voltage exceeds $\frac{2}{3}V_{cc}$, the upper comparator triggers. ✓
This causes the output to transition from HIGH to LOW.
In astable mode, the capacitor charges/discharges through this pin
In monostable mode, external timing networks connect here. (3)
- 4.4.2 Two comparators ✓
S/R flip-flop ✓ (2)
- 4.4.3 In astable mode, the 555 timer:
• Operates as a free-running oscillator. ✓
• Continuously switches between HIGH and LOW states. ✓
• No external trigger is required.
• Output frequency and duty cycle determined by timing resistors and capacitor.
• Produces a square wave output.
• Used in clock generation and timing applications. (2)
- 4.4.4 The pin closest to the dot. ✓
The pin to the left of the notch. ✓ (2)
- [25]

QUESTION 5: DIGITAL AND SEQUENTIAL DEVICES

- 5.1 LED (Light Emitting Diode) displays ✓
 LCD (Liquid Crystal Display) ✓
 Seven-segment displays
 16-segment displays
 Dot-matrix displays
 OLED displays
 Nixie tubes

(Any TWO) (2)

- 5.2 Current sinking ✓ digital output ✓

(2)

- 5.3 5.3.1 2-to-4 Line Decoder (or Binary Decoder) ✓

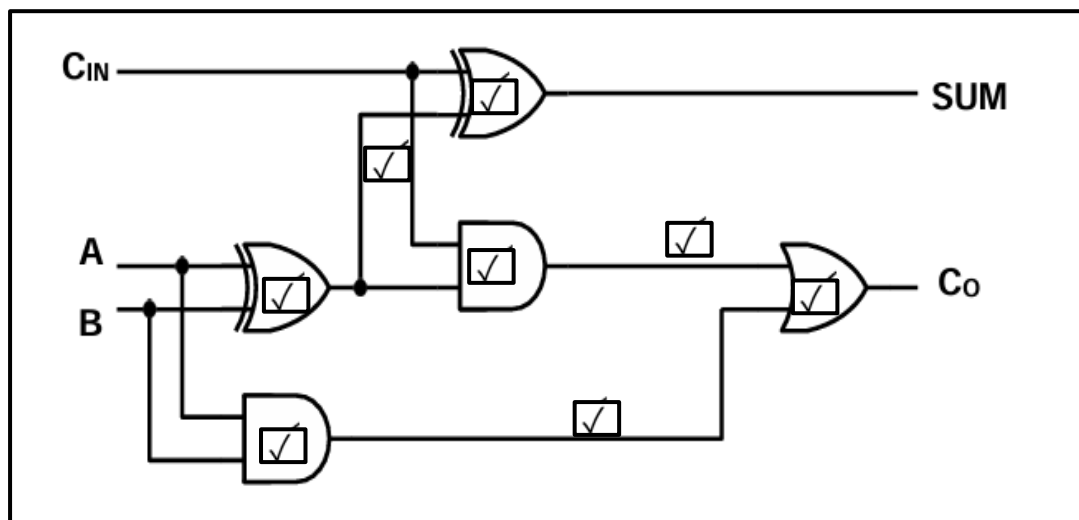
(1)

5.3.2

INPUTS		OUTPUTS			
A	B	W	X	Y	Z
0	0 ✓	1	0	0	0
0	1	0	1 ✓	0	0 ✓
1 ✓	0	0	0	1	0
1	1	0	0	0 ✓	1 ✓

(6)

5.4



(8)

- 5.5 5.5.1 The output of the first flip-flop ✓ feeds the clock pulse input of the next flip-flop. ✓

(2)

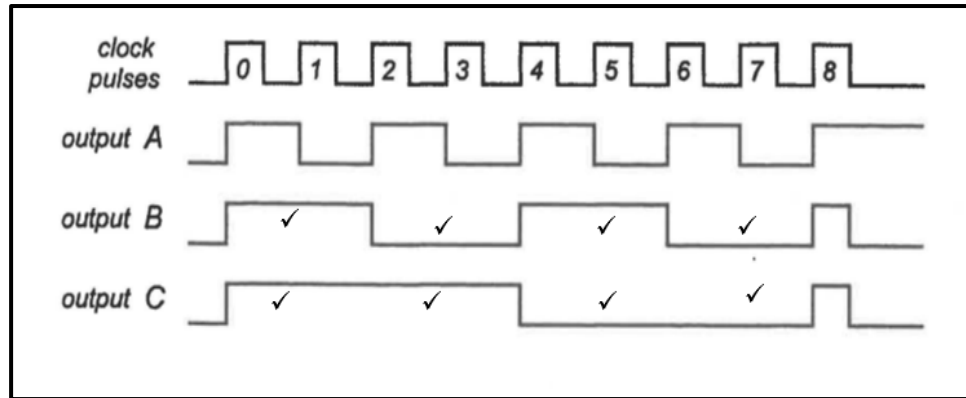
- 5.5.2 These are called asynchronous as they are not triggered at the same time ✓ therefore, the outputs will not change at the same time. ✓

(2)

- 5.5.3 $1 + 2 + 4 = 7$ ✓✓✓

(3)

5.5.4



(8)

5.6 5.6.1 D-type flip-flop (or D-latch) ✓

(1)

5.6.2 **Single Data Input (D):** ✓

- Unlike RS flip-flops with separate SET and RESET inputs, the D flip-flop has only one data input.
- This prevents conflicting commands to SET and RESET simultaneously.

Complementary Outputs: ✓

- Q and Q-bar (Q NOT) are always complementary (opposite states).
- Q-bar is the inverted output of Q.
- This ensures they cannot both be HIGH or both be LOW.

Clock Control: ✓

- All state changes are synchronized to the clock signal.
- Data is only transferred on clock edges.
- Prevents asynchronous transitions.

Internal Logic Design: ✓

- The cross-coupled NAND gate design ensures that only one output can be HIGH at any time
- Feedback paths maintain complementary states

(4)

5.6.3 Data storage and latching (holding data temporarily). ✓

Shift registers (serial data transfer). ✓

Frequency dividers (clock division).

State machine implementation.

Counters (binary counting).

Data capture and synchronization.

Delay circuits.

Multiplexing circuits.

(Any TWO answers) (2)

5.7 Combinational Logic Circuits:

Built from basic logic gates (AND, OR, NOT, XOR, NAND, NOR) ✓

Output depends ONLY on current inputs

No memory elements

Output changes immediately when inputs change

Examples: Adders, decoders, multiplexers, comparators

Sequential Logic Circuits:

Built from logic gates AND memory elements (flip-flops, latches) ✓

Output depends on current inputs AND previous states

Contains memory (flip-flops store previous states)

Output changes based on stored state and clock signal

Examples: Counters, shift registers, state machines

(Any TWO answers/comparisons)

(2)

5.8 Serial-in/Parallel-out (SIPO) – Data enters serially, exits in parallel ✓

Parallel-in/Serial-out (PISO) – Data enters in parallel, exits serially ✓

Parallel-in/Parallel-out (PIPO) – Data enters and exits in parallel

Bidirectional shift register – Data can shift left or right

Universal shift register – Can shift in both directions and load/unload data

(Any TWO answers)

(2)

5.9 5.9.1 A – Serial data in ✓

B – Clock ✓

(2)

5.9.2 The bits are loaded into the register one bit at a time ✓ usually from the left, moving the data from one flip-flop to the next flip flop ✓ for every clock pulse. ✓ This register will require 4 clock pulses to shift four bits in and 4 clock pulses to shift four bits out of the register. ✓ For example, a four-bit number such as 1111 will need four clock pulses to be loaded into the register and another four clock pulses for the number to move out in a serial manner. ✓

(5)

5.10 A truncated counter is a counter that counts up to a specific maximum value and then resets to zero, rather than counting through its full binary range. ✓

A standard 3-bit counter counts from 0 to 7 ($2^3 = 8$ states), while a truncated counter might count from 0 to 5, then reset to 0. ✓

(2)

5.11 Robotics ✓

Computer Numeric Control (CNC) machines.

(1)

[55]

QUESTION 6: MICROCONTROLLERS

- 6.1 6.1.1 Program Counter (PC) ✓
Memory Address Register (MAR) ✓
Memory Data Register (MDR) ✓
Current instruction Register (CIR) ✓ (4)
- 6.1.2 Stores intermediate results of arithmetic and logical operations ✓
Acts as the primary working register for the ALU (Arithmetic Logic Unit) ✓
Temporarily holds data being processed
Stores operands and results of calculations
Most frequently used register in CPU operations
Central to data manipulation tasks
(Any TWO answers) (2)
- 6.2 6.2.1 -200 mV represents ✓ Logic 0 (or LOW state)
+200 mV represents ✓ Logic 1 (or HIGH state) (2)
- 6.2.2 Point of sale (POS) terminals ✓
Metering instruments ✓
Industrial automation systems – Factory control and monitoring ✓
Building automation – HVAC, lighting, security systems
Power distribution networks – Smart grid communication
Weather stations – Remote sensor data collection
Parking lot systems – Vehicle detection and barriers
Fuel station monitoring – Tank level sensors
Traffic control systems – Traffic lights and vehicle detection
Renewable energy systems – Solar panel and wind turbine monitoring
Water treatment facilities – Level and flow monitoring
Elevator systems – Multi-floor building control
(Any THREE answers) (3)
- 6.2.3 Half-duplex: Where two devices ✓ takes turns in communicating, one after the other. ✓

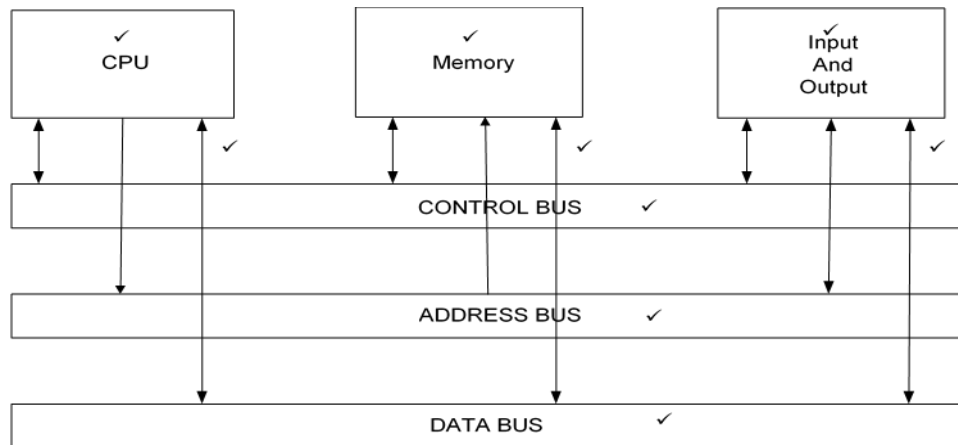
Full-duplex: Where two devices can both transmit and receive ✓ at the same time. ✓ (4)
- 6.3 6.3.1 A program is a sequence of instructions ✓ that tell a computer how to do a task. ✓

An algorithm is a precise set of procedures to be followed ✓ in order to solve a problem, being independent of any computer language. ✓ (4)
- 6.3.2 This process allows for a task to be repeated over and over. ✓ The task will be done repeatedly until the condition is true. ✓ (2)

6.4 6.4.1 Represents any type of Data input or output ✓ in a flow chart. ✓ (2)

6.4.2 Indicates the start or end of a program ✓ flow in the diagram. ✓ (2)

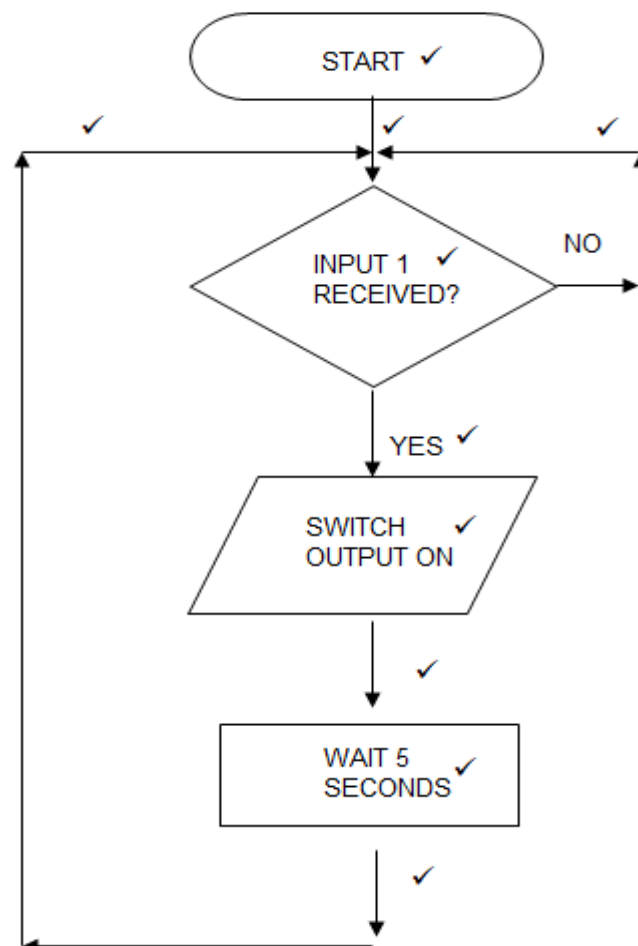
6.5 6.5.1



(9)

6.5.2 A shared boundary across which two separate components ✓ of a computer system exchange information. ✓ (2)

6.6



1 mark for each correctly placed label = 4

1 mark for each correctly placed flow line = 5

(9)

[45]

TOTAL:

200