



higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

NASIENRIGLYN

NATIONALE SERTIFIKAAT

LOGIKASTELSLS N3

24 November 2022

Hierdie nasienriglyn bestaan uit 8 bladsye.

VRAAG 1: GETALLESTEELSELS

1.1 $32,5_{16} + 32,5_8 + 32,5_{10}$

$$32,5_{16} = 00110010,0101_2 \checkmark$$

$$32,5_8 = 011010,101_2 \checkmark$$

$$32,5_{10} = 100000,1_2 \checkmark$$

$$\begin{array}{r} 110010,0101 \\ 011010,1010 \checkmark \\ \hline 100000,1000 \\ 1101101,0111 \checkmark \checkmark \end{array}$$

1.2 $1101101,0111_2 = 6D,7_{16} \checkmark$
 $55,5_{10} \times 2,3_8$

$$55,5_{10} = 110111,1_2 \checkmark$$

$$2,3_8 = 010,011_2 \checkmark$$

$$\begin{array}{r} 110111,100 \\ 10,011 \\ \hline 110111100 \\ 1101111000 \checkmark \checkmark \\ \hline 110111100000 \\ 10000011,110100 \checkmark \end{array}$$

$$10000011,1101_2 = 203,64_8 \checkmark$$

1.3 $C4,6_{16} - 2,4_8$

$$C4,6_{10} = 11000100,0110_2 \quad \checkmark$$

$$2,4_8 = 010,100_2 \quad \checkmark$$

$$\begin{array}{r}
 11000100,011 \\
 -00000010,100 \\
 \hline
 11111101,011 \\
 +1c \quad 11000100,011 \quad \checkmark \\
 \hline
 11000001,110 \quad \checkmark \\
 + \quad \quad \quad 1 \\
 \hline
 11000001,111 \quad \checkmark
 \end{array}$$

$$11000001,111_2 = 301,7_8 \quad \checkmark$$

1.4 $8C,4_{16} \div 5,4_8$

$$8C,4_{16} = 100001100,0100_2 \quad \checkmark$$

$$5,4_8 = 101,100_2 \quad \checkmark$$

$$\begin{array}{r}
 \overline{) 100011000,1} \quad 11001,1 \quad \checkmark \\
 \underline{1011} \\
 1101 \quad \checkmark \\
 \underline{1011} \\
 10000 \\
 \underline{1011} \\
 1011 \quad \checkmark \\
 \underline{1011} \\
 0
 \end{array}$$

$$11001,1_2 = 25,5_{10} \quad \checkmark$$

(4 × 5) **[20]**

VRAAG 2: KODES, DATA EN DATAKOMMUNIKASIE, ENKODEERDERS, DEKODEERDERS EN REKENKUNDIGE ELEMENTE

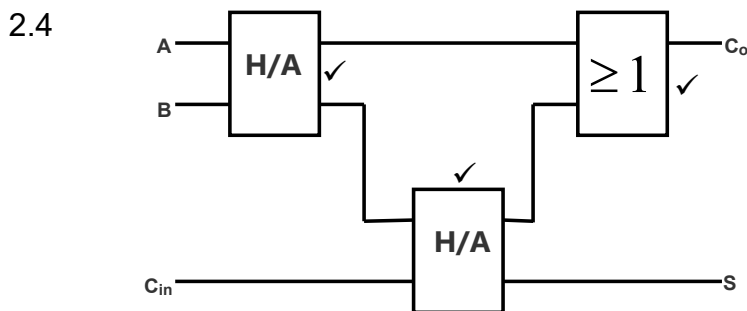
2.1 Amerikaanse Standaardkode vir Inligtingsuitruiling ('American Standard Code for Information Interchange') (2)

2.2 **8**
>
!
%
Q (5)

2.3 2.3.1 174_{10}
Binêr: 10101110_2 ✓
Gray: 11111001 ✓✓ (3)

2.3.2 57_{10} (2)

2.3.3 54_{10} (2)

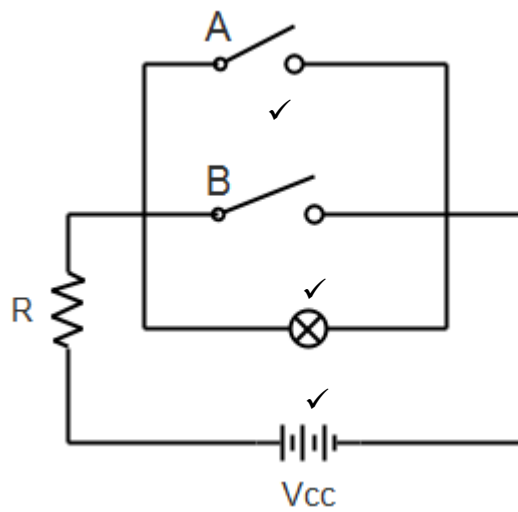


A	B	C_{in}	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(6)
[20]

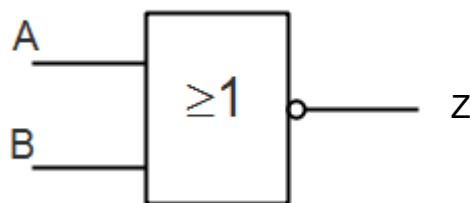
VRAAG 3: LOGIKAHEKKE, GEÏNTEGREERDE KRINGE EN LOGIKAFAMILIES

3.1 3.1.1



(3)

3.1.2



(1)

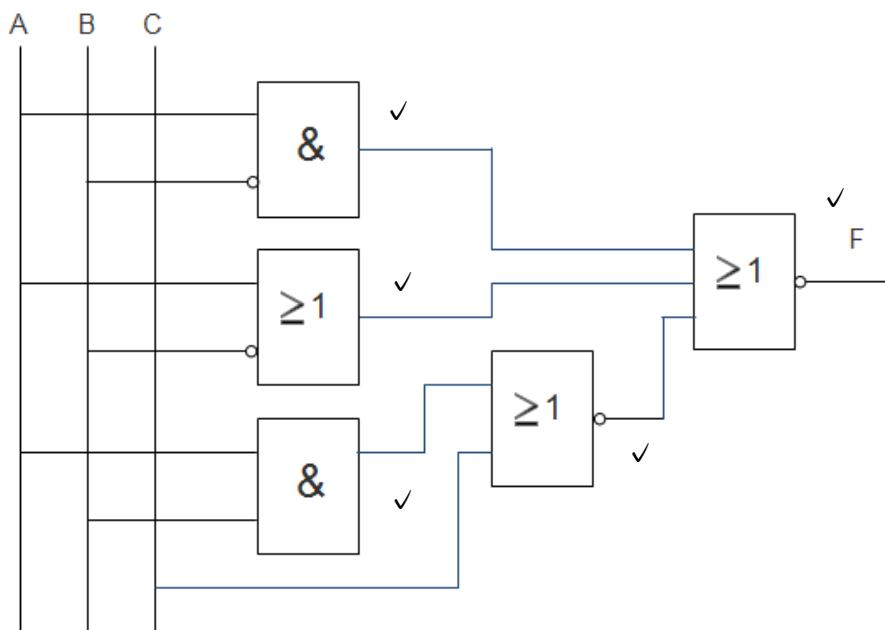
3.2

A	B	C	a	b	c	d	Z
0	0	0	1	1	1	1	0
0	0	1	1	0	0	1	0
0	1	0	1	0	0	1	0
0	1	1	1	0	0	1	0
1	0	0	1	0	0	1	0
1	0	1	1	0	0	1	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	1	1

✓ ✓ ✓ ✓ ✓

(5)

3.3



(5)

3.4 3.4.1 Die uitset van 'n inklusiewe OF-hek sal 'n logika 1 wees as enige van die insette of al die insette 'n logika 1 is.

3.4.2 Die uitset van 'n NEN-hek sal slegs 'n logika 0 wees as al die insette 'n logika 1 is. / Die uitset van 'n NEN-hek sal 'n logika 1 wees as enige van die insette of al die insette 'n logika 0 is.

3.4.3 Die uitset van 'n omkeerder sal 'n logika 1 wees as die inset 'n logika 0 is. / Die uitset van 'n omkeerder sal 'n logika 0 wees as die inset 'n logika 1 is.

(3 × 2)

(6)

[20]

VRAAG 4: GEHEUE-ELEMENTE EN GEHEUE

4.1 'n Houwipkring word gebruik om geheue of data te stoor.

(1)

4.2

A	B	Q	$\overline{Qn}$
0	0	Qn	$\overline{Qn}$
0	1	0	1
1	0	1	0
1	1	X	X

✓

(Geen
verandering)

✓

✓

✓

(Ongeldig)
(4)

[20]

5.1	5.1.1	Waar		
	5.1.2	Waar		
	5.1.3	Waar		
			(3 × 1)	(3)

The diagram illustrates a 4-bit shift register implemented with three J-K flip-flops and two AND gates. The flip-flops are labeled with 'Q' and 'Q-bar' outputs, 'J' and 'K' inputs, and a 'CL' (clock) input. The AND gates are represented by boxes with an ampersand (&). The circuit is connected as follows:

- The 'input' signal is connected to the 'J' input of the rightmost flip-flop and the 'K' input of the leftmost flip-flop.
- The 'CL' (clock) signal is connected to the 'CL' input of all three flip-flops.
- The 'Q' output of the leftmost flip-flop is connected to the 'J' input of the middle flip-flop.
- The 'Q' output of the middle flip-flop is connected to the 'J' input of the rightmost flip-flop.
- The 'Q-bar' output of the leftmost flip-flop is connected to the 'K' input of the middle flip-flop.
- The 'Q-bar' output of the middle flip-flop is connected to the 'K' input of the rightmost flip-flop.
- The 'Q' output of the rightmost flip-flop is connected to the 'Q(1)' output.
- The 'Q' output of the middle flip-flop is connected to the 'Q(2)' output.
- The 'Q' output of the leftmost flip-flop is connected to the 'Q(4)' output.
- The 'Q' output of the rightmost flip-flop is also connected to the 'Q' input of the AND gate that produces 'Q(1)'. The other input of this AND gate is the 'input' signal.
- The 'Q' output of the middle flip-flop is connected to the 'Q' input of the AND gate that produces 'Q(2)'. The other input of this AND gate is the 'input' signal.
- The 'Q' output of the leftmost flip-flop is connected to the 'Q' input of the AND gate that produces 'Q(4)'. The other input of this AND gate is the 'input' signal.

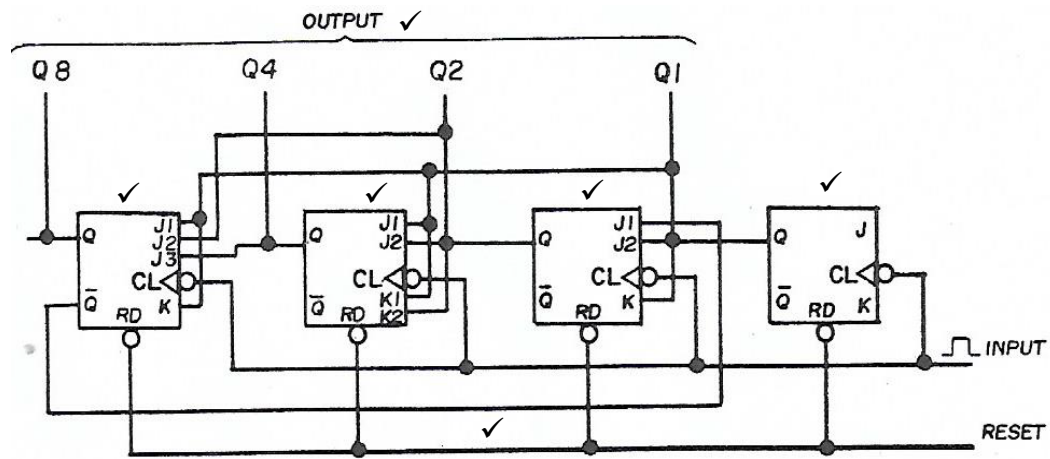
Checkmarks are placed above each flip-flop and each AND gate, indicating that they are correctly implemented.

Downloaded from www.mycourses.co.za

- 5.3 5.3.1 F
 5.3.2 B
 5.3.3 A
 5.3.4 E
 5.3.5 C

(5 × 1) (5)

5.4



(6)
[20]

TOTAAL: 100