



**higher education
& training**

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

NOVEMBER EXAMINATION

LOGIC SYSTEMS N3

25 NOVEMBER 2016

This marking guideline consists of 7 pages.

QUESTION 1

1.1 1.1.1

	8421	
F₁₆ =	1111	$\therefore F_{16} = 1111_2 \checkmark$

	421	421	
10₈ =	001	000	$\therefore 10_8 = 1000_2 \checkmark$

$$\begin{array}{r}
 \begin{array}{ccccccc}
 & & & 1 & 0 & 0 & 0 \\
 & & & \times & 1 & 1 & 1 & 1 \\
 \hline
 & & & 1 & 0 & 0 & 0 & \\
 & & 1 & 0 & 0 & 0 & & \checkmark \\
 & 1 & 0 & 0 & 0 & & & \\
 1 & 0 & 0 & 0 & & & & \\
 \hline
 1 & 1 & 1 & 1 & 0 & 0 & 0 & \checkmark
 \end{array}
 \end{array}$$

(4)

1.1.2

	8421	8421	
51₁₆ =	0101	0001	$\therefore 51_{16} = 1010001_2 \checkmark$

	8	4	2	1	
9₁₀ =	1	0	0	1	$\therefore 9_{10} = 1001_2 \checkmark$

$$\begin{array}{r}
 \begin{array}{cccc}
 1 & 0 & 0 & 1
 \end{array}
 \begin{array}{r}
 \begin{array}{ccccccc}
 & & & 1 & 0 & 0 & 1 & \checkmark \\
 1 & 0 & 1 & 0 & 0 & 0 & 1 & \\
 1 & 0 & 0 & 1 & \downarrow & \downarrow & \downarrow & \checkmark \\
 0 & 0 & 0 & 1 & 0 & \downarrow & \downarrow & \\
 & 0 & 0 & 0 & 0 & 0 & 0 & \checkmark \\
 & 0 & 0 & 1 & 0 & 0 & 1 & \\
 & & & 1 & 0 & 0 & 1 & \\
 & & & 0 & 0 & 0 & 0 &
 \end{array}
 \end{array}
 \end{array}$$

(5)

1.2

	7	1
71₈ =	111	001

$\therefore 71_8 = 111001_2 \checkmark$

2's complement of 111001 is equal to $000110 + 1 = 000111 \checkmark$

$$\begin{array}{r}
 0 \quad * \quad 1 \quad 0 \quad 1 \quad 0 \quad 1 \quad 1 \\
 1 \quad * \quad 0 \quad 0 \quad 0 \quad 1 \quad 1 \quad 1 \\
 \hline
 1 \quad * \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 1 \quad \checkmark
 \end{array}$$

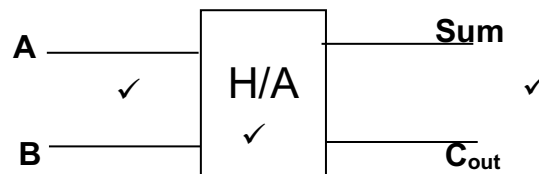
$\therefore$ two's complement of $1^* 110011$ is equal to $-001101 = -13_{10} \checkmark$ (4)

1.3 1.3.1 Adder $\checkmark \checkmark$ (2)

1.3.2 Half-adder $\checkmark$ (1)

1.3.3 Sum $\checkmark$ (1)

1.3.4



(3)
[20]

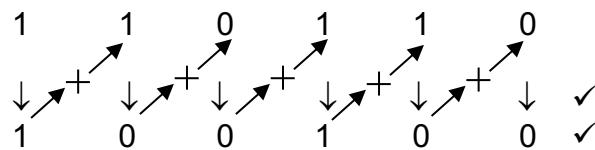
QUESTION 2

2.1 2.1.1 The purpose of a parity bit is to check the error $\checkmark$ and to protect the integrity of data being transmitted. $\checkmark$ (2)

2.1.2 The parity bit is added to a group of bits that are moved together. $\checkmark$ Before the bits are sent, they are counted and if the total number of data bits is even, $\checkmark$ the parity bit is set to one so that the total number of bits transmitted will form an odd number. $\checkmark$ If the total number of data bits is already an odd number, the parity bit remains or is set to zero. $\checkmark$ (4)

2.2 A word is the largest string of bits that a computer can handle in one operation, $\checkmark$ while word length is the number of bits in a word. $\checkmark$ (2)

2.3 2.3.1 11011 Gray to decimal



$$\therefore 100100_2 = 32 + 4 = 36_{10} \checkmark$$

(3)

2.3.2	1100	1010	0111
	↓	↓	↓
	12	10	7
	<u>-3</u>	<u>-3</u>	<u>-3</u>
	<u>9</u> ✓	<u>7</u> ✓	<u>4</u> ✓

(3)

2.4 N – 0110 1110✓
 u – 0111 0101✓
 m – 0110 1101✓
 b – 0110 0010✓
 e – 0110 0101✓
 r – 0111 0010✓

(6)
[20]**QUESTION 3**

3.1 3.1.1

FIGURE 2(a)		
A✓	B✓	X✓
0	0	0
0	1	0
1	0	0
1	1	1

FIGURE 2(b)		
A✓	B✓	Y✓
0	0	1
0	1	1
1	0	1
1	1	0

(6)

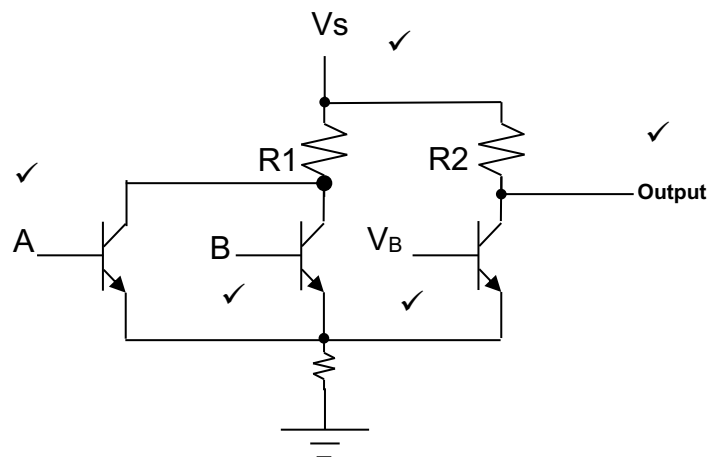
3.1.2 Output Y is the inverse of output X ✓✓

(2)

3.1.3 Figure 2(a) is an AND gate ✓
 Figure 2(b) is a NAND gate ✓

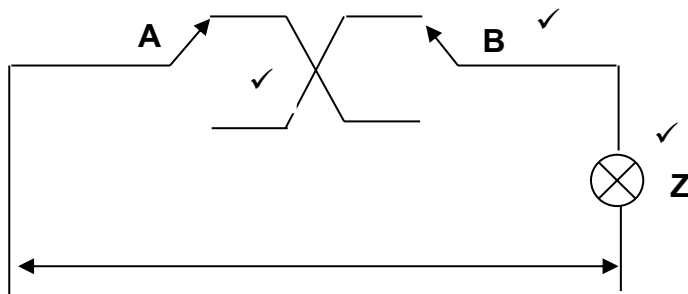
(2)

3.2



(5)

3.3



(3)

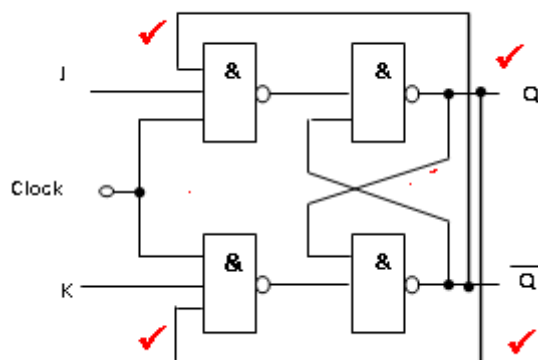
3.4 3.4.1 SSI – Small-scale integration

3.4.2 ECL – Emitter-coupled logic

(2 × 1)

(2)
[20]**QUESTION 4**

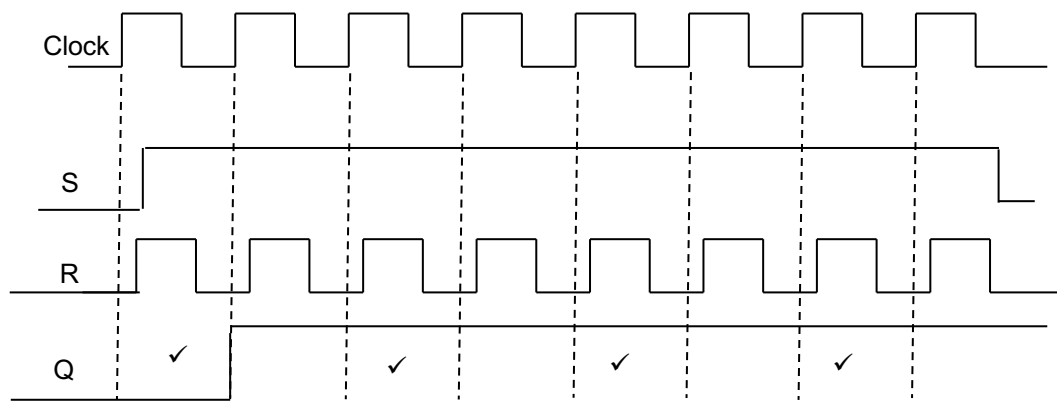
4.1



When $J = K = 0$ there will be no change in output Q . ✓ When $J = K = 1$ output Q will toggle meaning changing from one stage to another. ✓ When $J = 1$, $K = 0$ then output Q will be logic 1 ✓ and when $J = 0$ and $K = 1$ then output Q will be logic 0. ✓

(8)

4.2



(4)

4.3 4 GB = 4096 MB ✓✓

(2)

4..4

Main

- Semiconductor ✓
- Magnetic core ✓

Auxiliary

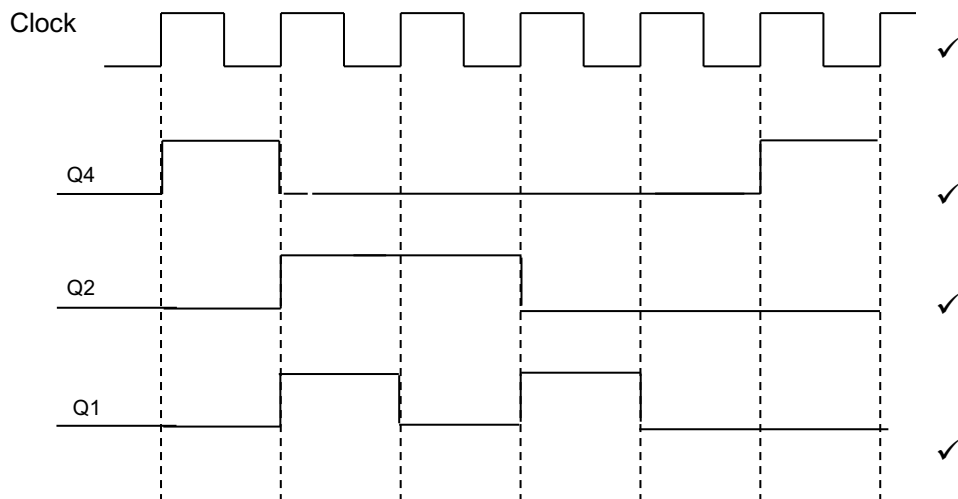
- Magnetic drum ✓
- Flash disk ✓
- Hard-drive ✓
- CD ROM ✓

(6)
[20]**QUESTION 5**

5.1	5.1.1	D
	5.1.2	C
	5.1.3	C
	5.1.4	B
	5.1.5	A
	5.1.6	B

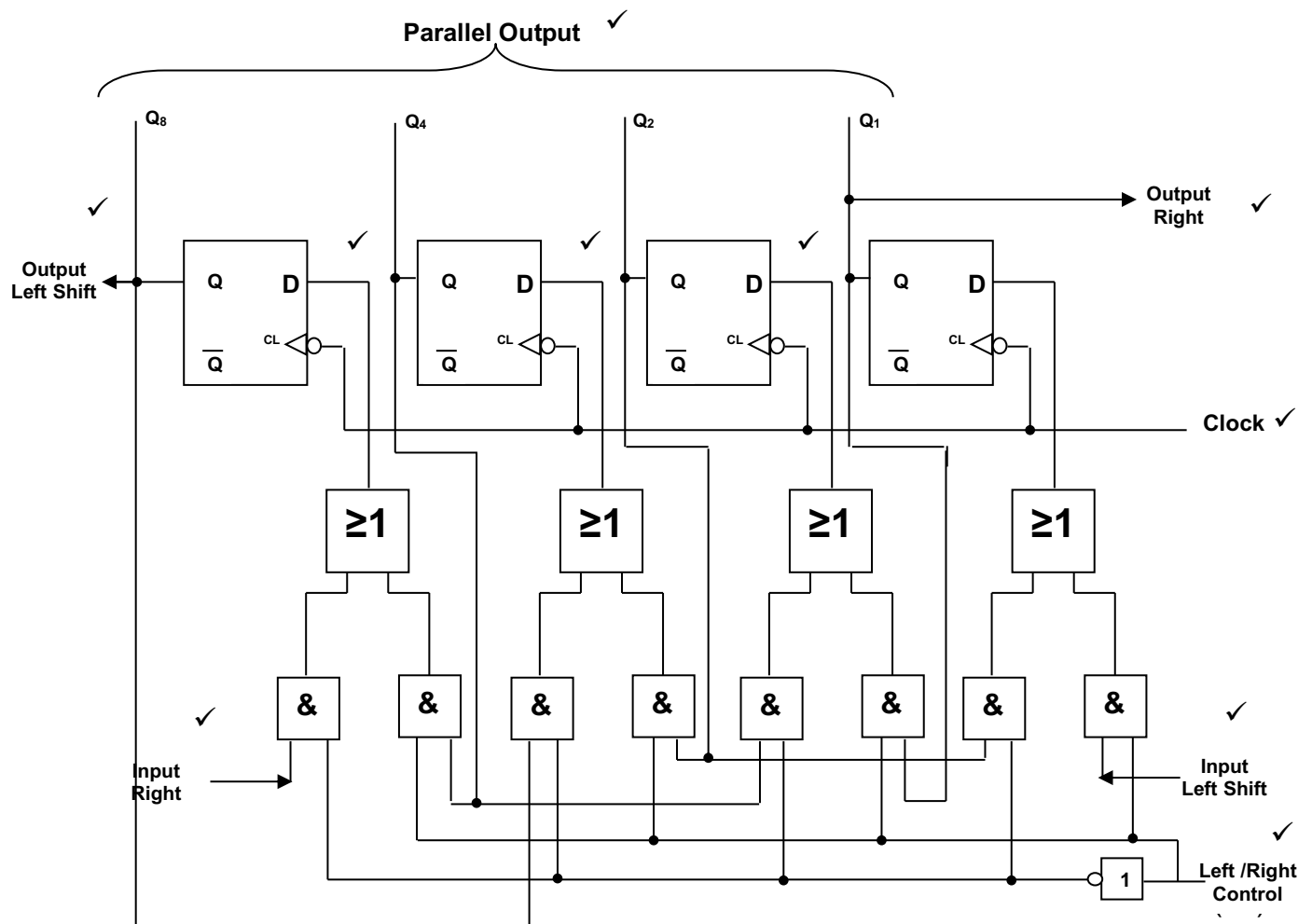
(6 × 1) (6)

5.2



(4)

5.3

(10)
[20]

TOTAL: 100