higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

1 AUGUST 2018

This marking guideline consists of 7 pages.

✓= 1 MARK ✓½ $= \frac{1}{2}$ MARK

QUESTION 1: NUMBER SYSTEMS AND ARITHMETIC ELEMENTS

1.1 14, 5_{10} + 4, 6_8 + 3, F_{16}

14, 5_{10} = 1 1 1 0, 1_2 ✓½
4, 6_8 = 1 0 0, 1 1 0_2 ✓½
3, F16 = 0 0 1 1, 1 1 1 1_2 ✓

	1	1	1	0	,	1	0	0	0	
	0	1	0	0	,	1	1	0	0	✓
	0	0	1	1	,	1	1	1	1	+
1	0	1	1	1	,	0	0	1	1	✓

14, 5_{10} + 4, 6_8 + 3, F_{16} = 1 0 1 1 1, 0 0 1 1_2 =27, 14_8 ✓

(5)

1.2 31,F_{16} - 31,2_8

31, F_{16} = 0 0 1 1 0 0 0 1, 1 1 1 1_2 ✓½
31, 2_8 = 0 1 1 0 0 1, 0 1 0_2 ✓½

	1	1	0	0	0	1	,	1	1	1	1	
	0	1	1	0	0	1	,	0	1	0	0	-
	1	1	0	0	0	1	,	1	1	1	1	
1'c	1	0	0	1	1	0	,	1	0	1	1	+ ✓
1	0	1	1	0	0	0	,	1	0	1	0	
											1	+ ✓
		1	1	0	0	0	,	1	0	1	1	✓

31, F_{16} - 31, 2_8 = 1 1 0 0 0, 1 0 1 1_2 = 24, 6875_{10} ✓ (5)

1.3 $6E,1_{16} \times 3,25_{10}$

$6E, 1_{16}$ = 1 1 0 1 1 1 0, 0 0 0 1_2 ✓½
$3, 251_0$ = 1 1, 0 1_2 ✓½

						1	1	0	1	1	1	0	,	0	0	0	1	
											1	1	,	0	1	0	0	×
	1	1	0	1	1	1	0	0	0	0	1	0	,	0	0	0	0	✓
		1	1	0	1	1	1	0	0	0	0	1	,	0	0	0	0	✓
				1	1	0	1	1	1	0	0	0	,	0	1	0	0	+ ✓
1	0	1	1	0	0	1	0	1	1	0	1	1		0	1	0	0	

$6E, 1_{16} \times 3, 25_{10}$ = 1 0 1 1 0 0 1 0 1, 1 0 1 1 0 1 0 0_2 = 165, $B4_{16}$ ✓ (5)

1.4 $A8, 7_{16} \div 13, 75_{10}$

$A8, 7_{16}$ = 1 0 1 0 1 0 0 0, 0 1 1 1_2 ✓½
$13, 75_{10}$ = 1 1 0 1, 1 1_2 ✓½

										1	1	0	0	,	0	1	✓
1	1	0	1	1	1	1	0	1	0	1	0	0	0	1	,	1	1	
						-	1	1	0	1	1	1						
								1	1	1	0	1	0					✓
							-	1	1	0	1	1	1					
											1	1	0	1		1	1	✓
										-	1	1	0	1		1	1	
											0	0	0	0		0	0	

$A8, 7_{16} \div 13, 75_{10}$ = 1 1 0 0, 0 1_2 = 12, 25_{10} ✓

(5)
[20]

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS AND DECODERS

2.1 A parity bit is used for error detection✓ and correction.✓ (2)

2.2 An encoder is used to convert a decimal code✓ to a binary or BCD code.✓ (2)

2.3 The decoder starts decoding from 0000 (0)✓ right up to 1111 (9) which shows that it decodes ten times.✓ (2)

2.4 2.4.1 316_{10} = 0 0 1 1 0 0 0 1 0 1 1 0_2 ✓✓✓

= 0 0 1 1 + 0 0 1 1 + 0 0 1 1 +

= 0 1 1 0 0 1 0 0 1 0 0 1$_{XS3}$

or 3 1 6 + 3 3 3 + = 6 4 9

0 1 1 0 0 1 0 0 1 0 0 1$_{XS3}$ ✓✓✓

2.4.2 10011101

$=11101001_2$ Binary ✓

$=233_{10}$ ✓

=0010 0011 0011 ✓: 8421BCD

(2 × 3) (6)

2.5

1	1	1	0	1	0	1	1	E
1	1	0 ✓	1	1	1	0	0	U ✓
1	0	1	1	1	1	0	1	E
1	0	0	1	0	0	1	1	E
1	1	1	1	0	0	1	1	E
1	1	0	0	1	0	1	0	E
E	E	U ✓	E	E	E	E	E	✓ ✓

The fault is in column 3, row 2. The 0 is changed to a 1. ✓

1 1 **1** 0 1 0 1 1
1 1 1 1 1 1 0 0✓
1 0 **1** 1 1 1 0 1
1 0 **0** 1 0 0 1 1
1 1 **1** 1 0 0 1 1
1 1 **0** 0 1 0 1 0✓

(8)
[20]

QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES

3.1
3.1.1 False
3.1.2 True
3.1.3 False
3.1.4 True
3.1.5 False

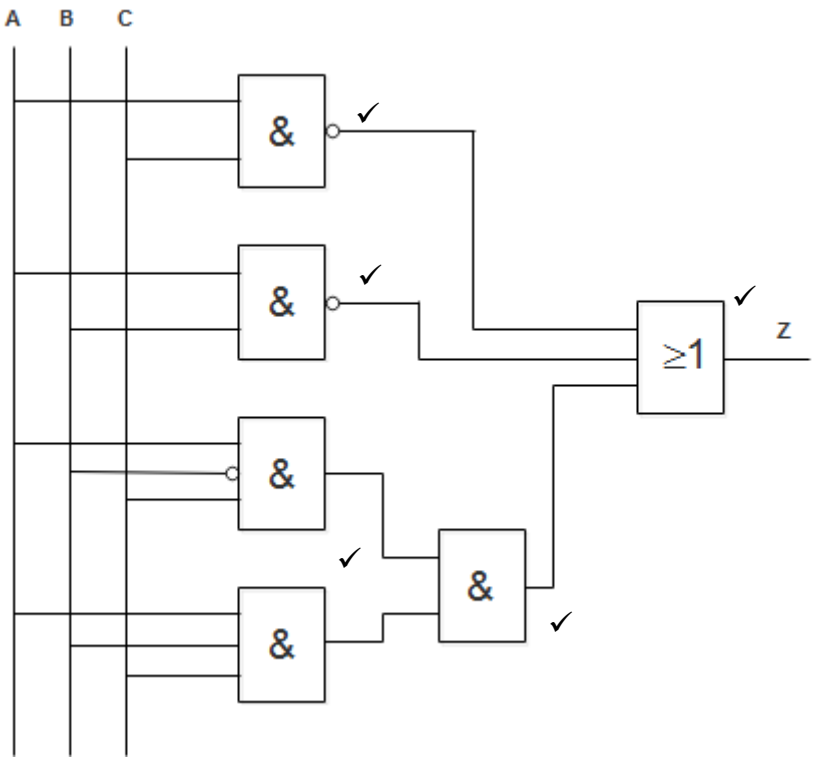
(5 × 1) (5)

3.2

A	B	C	a	b	c	d	Z
0	0	0	0	0	0	0	1
0	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0
0	1	1	0	1	0	1	0
1	0	0	0	1	0	1	0
1	0	1	0	1	0	1	0
1	1	0	1	1	0	1	0
1	1	1	0 ✓	1 ✓	1 ✓	1✓	1 ✓

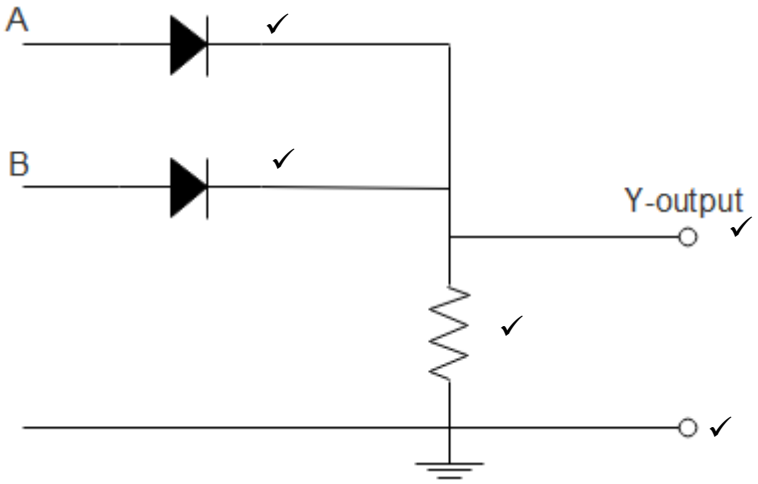
(5)

3.3



(5)

3.4



(5)
[20]

QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1
4.1.1 B
4.1.2 A
4.1.3 B
4.1.4 A
4.1.5 B

(5 × 1) (5)

4.2 CD-R cannot be erased once data is written on it, while CD-RW can be erased and reused. (2)

4.3

MAIN MEMORY	SECONDARY MEMORY
Magnetic core memory✓ Semiconductor memories✓	Paper tape✓ Floppy disc✓ <u>Alternate answers</u> Punch card Compact disc DVD Flash disc

(2 × 2) (4)

4.4
4.4.1 The minimum time for which the voltage levels at the excitation inputs must remain constant ✓ after the triggering edge of the clock pulse, in order for the levels to be reliably clocked into the flip-flop ✓

4.4.2 When the flip-flop changes state either at the positive or negative edge ✓ of the clock pulse and it is sensitive to its inputs only at this transition of the clock ✓

4.4.3 The time required to change ✓ the voltage level from 10% to 90% ✓

(3 × 2) (6)

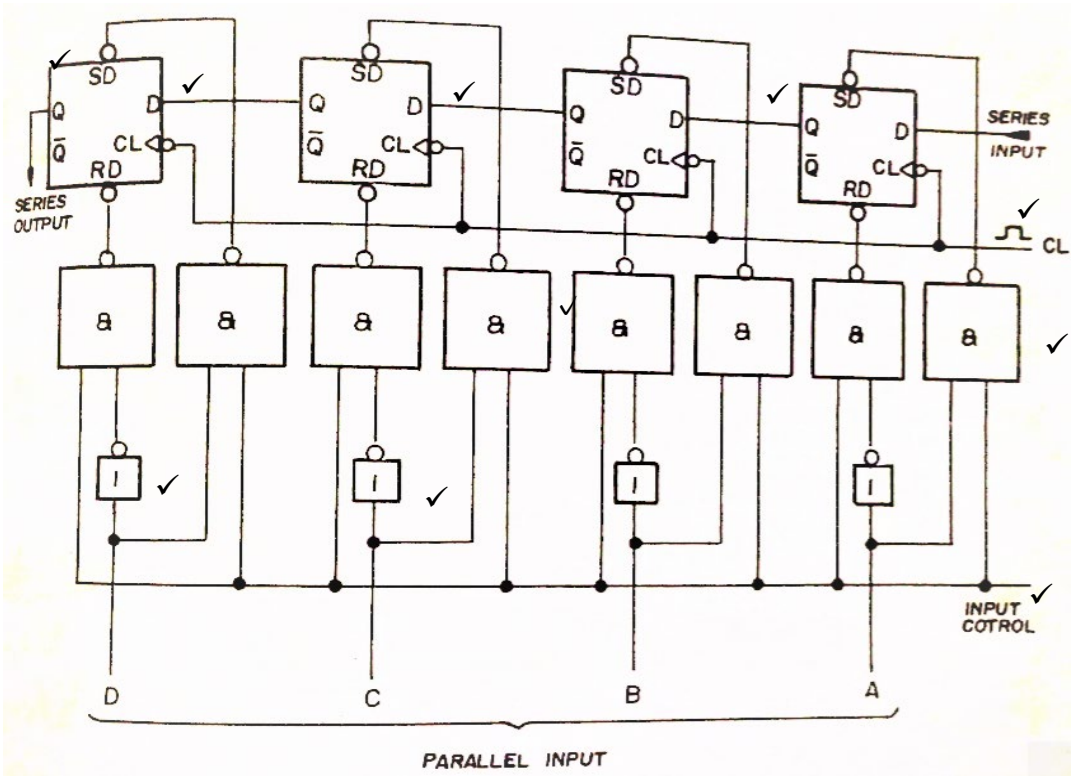
4.5 Flash memories are high-density read/write memories ✓ that are non-volatile, ✓ which means data can be stored indefinitely without power. ✓ (3)
[20]

QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1
5.1.1 C
5.1.2 D
5.1.3 C
5.1.4 C
5.1.5 A

(5 × 1) (5)

5.2



(10)

5.3 Synchronous counters✓ are faster because flip-flops are clocked simultaneously or in parallel.✓✓ (3)

5.4 A JK flip-flop has more control options than a D flip-flop. ✓
A JK flip-flop can function as a D flip-flop by tying JK together and calling the node 'D'. ✓ (2)
[20]

TOTAL: 100