



higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T860(E)(A6)T
NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

(8080273)

6 April 2018 (X-Paper)
09:00–12:00

Calculators may not be used.

This question paper consists of 8 pages.

DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA
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LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
 2. Read ALL the questions carefully.
 3. Number the answers according to the numbering system used in this question paper.
 4. Keep questions and subsections of questions together.
 5. ALL the sketches and diagrams must be large, clear and neat.
 6. Show ALL the steps and calculations.
 7. Write neatly and legibly.
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QUESTION 1: NUMBER SYSTEMS AND ARITHMETIC ELEMENTS

Convert each of the following numbers to its binary equivalent, complete the calculation in the binary number system and then complete the instructions. Show ALL conversions.

1.1 $4A,6_{16} + 3,7_8 + 5,25_{10}$

Convert the final answer to the hexadecimal system. (5)

1.2 $A,B7_{16} - 3,2_8$

Make use of the one's complement method and convert the final answer to the octal system. (5)

1.3 $110,5_{10} \times 1,2_8$

Convert the final answer to the hexadecimal system. (5)

1.4 $86,2_{16} \div 7,25_{10}$

Convert the final answer to the decimal system. (5)
[20]

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS AND DECODERS

2.1 Draw a neat labelled diagram of a 2421 BCD encoder. (8)

2.2 Encode the following to the code/number as indicated:

2.2.1 $100111011100_{2421BCD}$ to decimal

2.2.2 425_{10} to the Gray code (2 × 3) (6)

2.3 Decode the following word which is in the ASCII code:

100 0100
100 1001
100 0111
100 1001
101 0100
101 0011

(6)
[20]

QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES

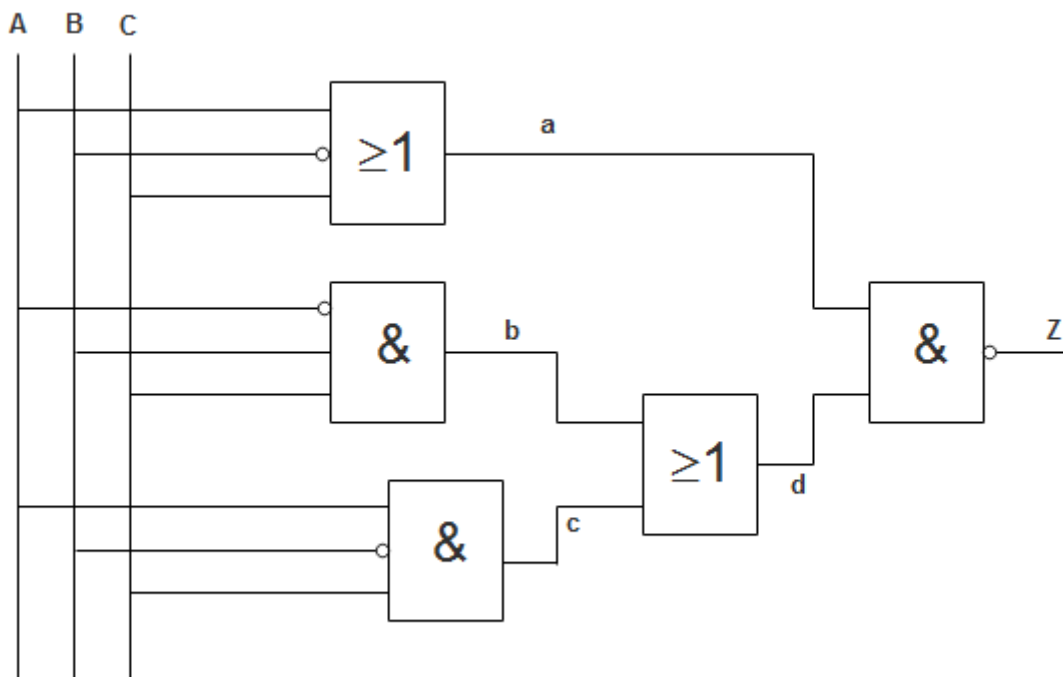
3.1 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (3.1.1–3.1.5) in the ANSWER BOOK.

- 3.1.1 A NAND gate output is LOW only if all the inputs are HIGH.
- 3.1.2 A logic gate has one or more output terminals and one input terminal.
- 3.1.3 An OR array is programmed by blowing fuses to eliminate selected variables from the output functions.
- 3.1.4 An exclusive-NOR gate output is HIGH when the inputs are unequal.
- 3.1.5 An inverter output is the complement of its input.

(5 × 1)

(5)

- 3.2 Below is a circuit diagram that consists of AND gates, OR gates and a NAND gate.



Copy and complete the truth table for the circuit.

A	B	C	a	b	c	d	Z
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

(5)

- 3.3 Make a neat, labelled sketch of the circuit diagram of the Boolean expression below without changing or simplifying the expression.

$$Z = (A+B)(A+C) + ABC\bar{C}$$

(5)

- 3.4 List FIVE bipolar logic families.

(5)
[20]

QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (4.1.1–4.1.5) in the ANSWER BOOK.

- 4.1.1 A major disadvantage of the mask ROM is that it ...
- A is time-consuming to change the stored data when system requirements change.
 - B is very expensive to change the stored data when system requirements change.
 - C cannot be reprogrammed if stored data needs to be changed.
 - D has an extremely short life expectancy and requires frequent replacement.
- 4.1.2 Which type of ROM can be erased by UV light?
- A ROM
 - B Mask ROM
 - C EPROM
 - D EEPROM
- 4.1.3 How many $1K \times 4$ RAM chips would be required to build a $1K \times 8$ memory system?
- A 2
 - B 4
 - C 8
 - D 16
- 4.1.4 Which ONE of the following memories is volatile?
- A ROM
 - B EROM
 - C RAM
 - D Flash
- 4.1.5 How can UV erasable PROMs be recognised?
- A There is a small window on the chip.
 - B They will have a small violet dot next to the #1 pin.
 - C Their part number always starts with a U, such as in U12.
 - D They are not readily identifiable, since they must always be kept under a small cover.

(5 × 1) (5)

- 4.2 Write down the following abbreviations in full:
- 4.2.1 CD – RW
- 4.2.2 CD –R
- (2 × 2) (4)
- 4.3 Draw a logic circuit for a clocked JK flip-flop and explain what happens to output Q when clocked if J = K = 0; J = K = 1; and J = 1 and K = 0. (7)
- 4.4 Explain the difference between a *combinational* and a *sequential* circuit. (4)
- [20]**

QUESTION 5: SHIFT REGISTERS AND COUNTERS

- 5.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (4.1–4.10) in the ANSWER BOOK.
- 5.1.1 The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains ...
- A 10111000.
B 10110111.
C 11110000.
D 11111100.
- 5.1.2 When an 8-bit serial in/serial out shift register is used for a 20s-time delay, the clock frequency is ...
- A 40 kHz.
B 50 kHz.
C 400 kHz.
D 500 kHz.
- 5.1.3 Ring shifts and Johnson counters are ...
- A synchronous counters.
B asynchronous counters.
C true binary counters.
D synchronous and true binary counters.
- 5.1.4 Computers operate on data internally in a ... format.
- A tristate
B universal
C parallel
D serial

5.1.5 How much storage capacity does each stage in a shift register represent?

- A One bit
- B Two bits
- C Four bits (one nibble)
- D Eight bits (one byte)

(5 × 1) (5)

5.2 A universal shift register is an integrated logic circuit that can shift in both directions, namely from left to right and from right to left. This register has parallel load capacity as well.

Draw the circuit of a universal shift register. (10)

5.3 Draw the truth table as well as the timing diagram for a module 5-up-counter. Use FIVE clock pulses. (5)

[20]

TOTAL: 100