

# **MARKING GUIDELINE**

**NATIONAL CERTIFICATE**

**APRIL EXAMINATION**

**LOGIC SYSTEMS N3**

**7 APRIL 2015**

**This marking guideline consists of 7 pages.**

1.1.8 C ✓

1.2

1.2.1 False ✓  
1.2.2 True ✓  
1.2.3 False ✓ ✓  
1.2.4 True ✓  
1.2.5 False ✓  
1.2.6 False ✓  
1.2.7 True ✓  
1.2.8 True ✓  
1.2.9 False ✓

(1)  
(1)  
(2)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)

1.3

1.3.1 C  
1.3.2 E  
1.3.3 B  
1.3.4 D  
1.3.5 A

(5 × 1)

(5)  
[25]

TOTAL SECTION A: 25

$$(7 \times 16^1) + (8 \times 16^0) = 112 + 8 = 120_{10} \checkmark$$

Ten's complement of 120 is  $1\ 000 - 120 = 880 \checkmark$

$$\begin{array}{r} 0 \quad * \quad 1 \quad 5 \quad 1 \\ 1 \quad * \quad 8 \quad 8 \quad 0 \\ \hline 1 \quad 0 \quad * \quad 0 \quad 3 \quad 1 \quad \checkmark \end{array}$$

↳ ignore carry

(4)

$$2.2 \quad 37_8 \times 1000_2$$

|     |     |
|-----|-----|
| 3   | 7   |
| 011 | 111 |

$$\therefore 37_8 = 11111_2 \checkmark$$

$$\begin{array}{r} 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \\ 1 \quad 1 \quad 0 \quad 0 \quad 0 \quad 0 \\ \hline 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\ 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\ 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\ \hline 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \\ 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \\ \hline 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 0 \quad 0 \quad 0 \quad 0 \quad \checkmark \end{array}$$

|     |    |    |    |   |   |   |   |
|-----|----|----|----|---|---|---|---|
| 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 1   | 1  | 1  | 1  | 1 | 0 | 0 | 0 |

$$\therefore 11111000 = 128 + 64 + 32 + 16 + 8 = 248_{10} \checkmark$$

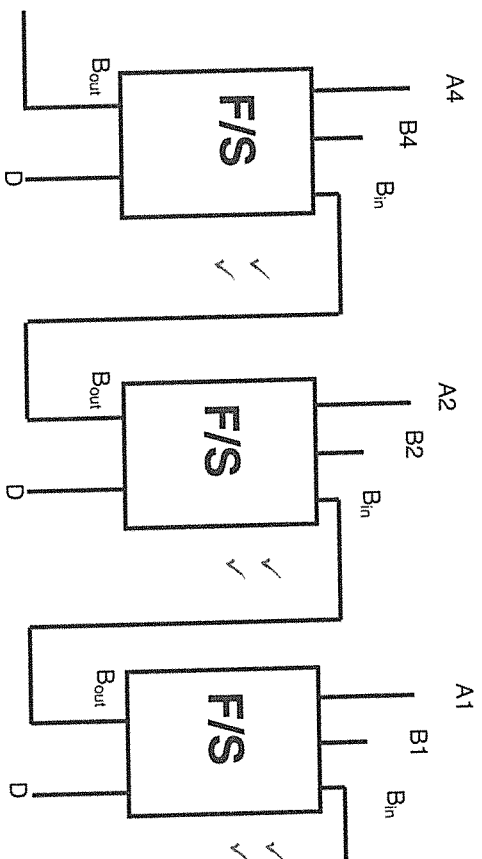
(4)

|   |   |   |   |
|---|---|---|---|
| 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 |

$$\therefore 1010_2 = A_{16} \checkmark$$

(4)

## 2.4 3-bit parallel subtractor.



(6)

## 2.5

21 to XS3

|      |      |
|------|------|
| 2    | 1    |
| +3   | +3   |
| 5    | 4    |
| ↓ ✓  | ↓ ✓  |
| 0101 | 0100 |

OR

|        |        |
|--------|--------|
| 2      | 1      |
| ↓      | ↓      |
| 0010   | 0001   |
| + 11   | + 11   |
| 0101 ✓ | 0100 ✓ |

(2)

## 2.6

100 0001 → A ✓  
 101 0011 → S ✓  
 100 0011 → C ✓  
 100 1001 → I ✓  
 100 1001 → I ✓

(5)

|   |   |   |   |   |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 9 |
|---|---|---|---|---|

(2)  
[30]

QUESTION 3

3.1 3.1.1

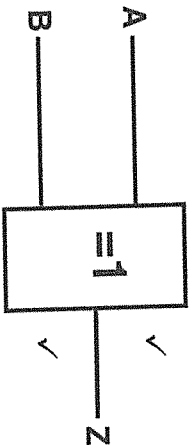
| Inputs |   | Outputs |    |    |    |
|--------|---|---------|----|----|----|
|        |   | ✓✓      | ✓✓ | ✓✓ | ✓✓ |
| A      | B | X       | Y  | Z  |    |
| 0      | 0 | 0       | 0  | 0  |    |
| 0      | 1 | 0       | 1  | 1  |    |
| 1      | 0 | 1       | 0  | 1  |    |
| 1      | 1 | 0       | 0  | 0  |    |

(6)

3.1.2 Exclusive OR (XOR) gate ✓✓

(2)

3.1.3



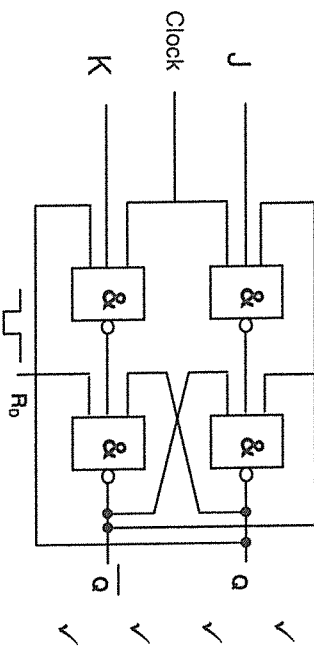
(2)

3.2 Advantage: bipolar IC has higher speed/it is faster than MOS IC. ✓✓  
Disadvantage: bipolar IC uses more power than MOS IC. ✓✓

(4)

3.3 12 ✓

(1)  
[15]



If  $J = K = 0$  and clock pulse is applied to the flip-flop, the output will remain unchanged ✓

If  $J = K = 1$ , then the output will toggle (switch over to the opposite position with every clock pulse); and ✓

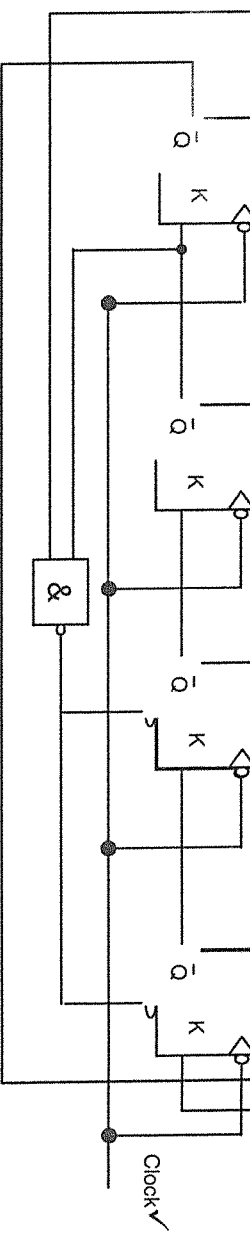
If  $J = 1, K = 0$ , then the 1 will be carried over to the output by a clock pulse ✓ (7)

4.3 4.3.1 CD-RW stands for rewritable compact disc. ✓ ✓

4.3.2 CD-R stands for recordable compact disc. ✓ ✓

(2 × 2)

(4)  
[15]



5.3.1 1010, 1011, 1110 and 1111 (5)

5.3.2 0011 (Or ANY four-bit binary number. Why? Because the initial content of the down-counter is UNKNOWN.)✓✓ (2)

[15]

TOTAL SECTION B: 75  
GRAND TOTAL: 100