

# **MARKING GUIDELINE**

## **NATIONAL CERTIFICATE APRIL EXAMINATION LOGIC SYSTEMS N3 1 APRIL 2014**

**This marking guideline consists of 7 pages.**

1.1.8 C ✓ (1)  
1.1.9 D ✓ (1)

1.2  
1.2.1 False  
1.2.2 False  
1.2.3 True  
1.2.4 True  
1.2.5 True  
1.2.6 False  
1.2.7 False  
1.2.8 True  
1.2.9 False  
1.2.10 True

(10 x 1) (10)

1.3  
1.3.1 C  
1.3.2 A  
1.3.3 D  
1.3.4 E  
1.3.5 B

(5 x 1) (5)

TOTAL SECTION A: 25

(4)

2.2

|               | P1   | P2   | D1   | P3   | D2   | D3   | D4   | P4   | D5   |  |
|---------------|------|------|------|------|------|------|------|------|------|--|
| Positions     | 1    | 2    | 3    | 4    | 5    | 6    | 7    | 8    | 9    |  |
| Binary values | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 |  |
| Word          | 0    | 1    | 1    | 0    | 0    | 1    | 1    | 0    | 0    |  |

✓

✓

|          |   |   |   |   |   |   |   |   |   |     |
|----------|---|---|---|---|---|---|---|---|---|-----|
| Parity 1 | 0 |   | 1 |   | 0 |   | 1 |   | 0 | = 0 |
| Parity 2 |   | 1 | 1 |   |   | 1 | 1 |   |   | = 0 |
| Parity 3 |   |   |   | 0 | 0 | 1 | 1 |   |   | = 0 |
| Parity 4 |   |   |   |   |   |   |   | 0 | 0 | = 0 |

✓

✓

✓

Fault is on position zero(0000), which means that there is no fault on the transmitted word ✓

(7)

2.3

| C    | F    |
|------|------|
| 1100 | 1111 |

$$\therefore CF_{16} = 11001111_2 \checkmark$$

$$\text{One's complement of } 00110000 = 11001111 \checkmark$$

$$\begin{array}{r}
 \begin{array}{cccccccccccc}
 1 & 0 & * & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 \\
 \swarrow & & & & & & & & & & & \\
 0 & * & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \\
 1 & * & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \\
 \hline
 1 & 0 & * & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & \checkmark \\
 \downarrow & & & & & & & & & & & \\
 1 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & & \checkmark
 \end{array}
 \end{array}$$

$$\therefore 10\ 011\ 111 = 237_8 \checkmark$$

(5)

$$1001101_2 = 233_8 \checkmark$$

$$\omega$$

### 2.4.2

|   |   |   |   |
|---|---|---|---|
| 8 | 4 | 2 | 1 |
| 1 | 0 | 1 | 0 |

$$\therefore 10_{10} = 1010_2 \checkmark$$

[illegible]

|   |   |   |   |
|---|---|---|---|
| 8 | 4 | 2 | 1 |
| 1 | 1 | 1 | 1 |

$$\therefore 11111_2 = 15_{10} \checkmark$$

(4)

## 2.5

### 2.5.5.1

|      |      |      |
|------|------|------|
| 4221 | 4221 | 4221 |
| 1100 | 0011 | 1111 |
| ↑    | ↑    | ↑    |
| 6    | 3    | 9    |

### 2.5.5.2

[illegible]

| Binary string  | 4221 BCD | Gray code        |
|----------------|----------|------------------|
| 1100 0011 1111 | 639✓✓    | 101000100000✓✓✓✓ |

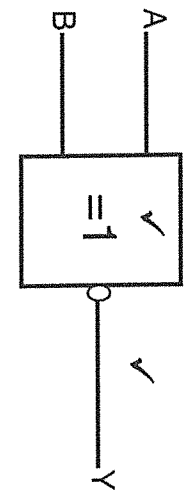
(7)  
[30]

3.1.4 NOR gate ✓✓ (3)

3.1.5 DTL or Diode Transistor Logic ✓ (2)

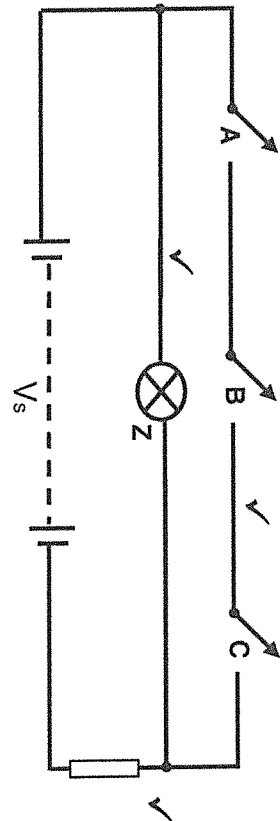
(1)

3.2



(2)

3.4 Three-input NAND gate.



(3)  
[15]

QUESTION 4

4.1

| POSITIONS | MASTER  | SLAVE   |
|-----------|---------|---------|
| 1         | Closed✓ | Open✓   |
| 2         | Closed✓ | Closes✓ |
| 3         | Opens✓  | Closed✓ |
| 4         | Closes✓ | Closed✓ |
| 5         | Closed✓ | Opens✓  |
| 6         | Closed✓ | Open✓   |

(6)

4.3.2 SRAM ✓ and DRAM ✓

(2)

4.3.3 RAMs are called volatile memories because RAMs lose stored data when the power is turned OFF. ✓✓

(2)  
[15]

## QUESTION 5

5.1 A "register" is a collection of flip-flops or latches used to store a binary number; it is a one-word memory circuit. ✓✓ A shift register differs because it is a register that is used to shift binary words from one direction to another. ✓✓ (4)

5.2 Because an output of one flip-flop is a clock of the next one ✓✓ (2)

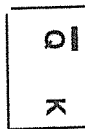
5.3 Serial-In, Serial-Out Shift Register ✓  
Serial-In, Parallel-Out Shift Register ✓  
Parallel-In, Serial-Out Shift Register ✓  
Parallel-In, Parallel-Out Shift Register ✓  
Bidirectional Shift Register (Any applicable 4 × 1) (4)

R

Clock



S



Q

(5)  
[15]

TOTAL SECTION B: 75  
GRAND TOTAL: 100