higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T840(**E**)(A9)T
APRIL EXAMINATION

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

(8080262)

9 April 2014 (Y-Paper)
13:00–16:00

Calculators may NOT be used.

This question paper consists of 6 pages.

DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N2
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Write neatly and legibly.

SECTION A

QUESTION 1

1.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (1.1.1–1.1.5) in the ANSWER BOOK.

1.1.1 To turn an OR gate into a NOR gate we must add a …

A NAND gate.
B A second OR gate.
C NOR gate.
D NOT gate.

1.1.2 An XOR gate will give a logic 1 output if …

A all the inputs are logic 1.
B any of the input is logic 1.
C one input is the inverse of the other one.
D all the inputs are logic 0.

1.1.3 The D-input on a D-type flip flop is the …

A delta input.
B drain input.
C data input
D dee input

1.1.4 Shift registers are made from …

A T-type flip flops
B D-type flip flops
C J-K flip flops
D S-R flip flops

1.1.5 A half-adder will add decimal numbers up to …

A one-half.
B one.
C two.
D three.

(5 x 1) (5)

1.2 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (1.2.1–1.2.5) in the ANSWER BOOK.

1.2.1 A ripple counter is an synchronous counter.

1.2.2 Bidirectional shift registers can shift data either right or left.

1.2.3 An output of an exclusive-OR (XOR) gate is 1 only when the inputs are different.

1.2.4 ROMs are volatile.

1.2.5 A T-type flip-flop is constructed by connecting an inverter between the set and the clock terminals.

(5 x 1) (5)
[10]

TOTAL SECTION A: 10

SECTION B

QUESTION 2

2.1 List FOUR binary subtraction rules. (4)

2.2 What is meant by *self-complementing code*? Give an example of a self-complementing code. (3)

2.3 Convert each of the following decimal numbers to their binary equivalents and then complete the calculations in the binary number system:

2.3.1 25 + 31 + 10 (4)

2.3.2 120 ÷ 15 (4)

2.4 calculate the following numbers in binary number systems and convert the final answer to the decimal number system:

2.4.1 111110 – 11011 (3)

2.4.2 110 × 1111 (4)

2.5 Draw an IEC symbol for a half-subtractor and also draw the truth table. (6)

2.6 Convert the following numbers to the indicated code:

2.6.1 111100111100 2421 BCD code to its decimal equivalent. (3)

2.6.2 60 to its binary XS3 equivalent. (2)

2.7 Draw a neat, labelled logic circuit for an 8421 BCD decoder. (7)
[40]

QUESTION 3

3.1 Study the switch circuits below and answer the questions:

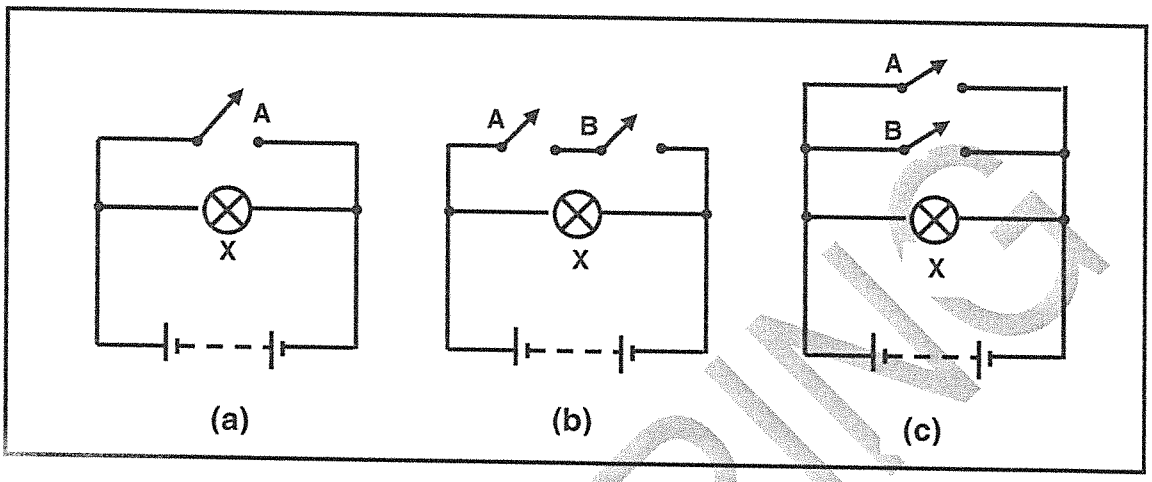

FIGURE 1

3.1.1 Identify the names of the gates represented in FIGURE 1 above. (3)

3.1.2 Draw the IEC symbol for the gate represented by FIGURE 1 (b) above. (2)

3.1.3 Draw the truth table for the gate represented by FIGURE 1(c) above. (3)

3.1.4 Define the gate represented by FIGURE 1(a) above. (2)

3.2 Study FIGURE 2 below and answer the questions:

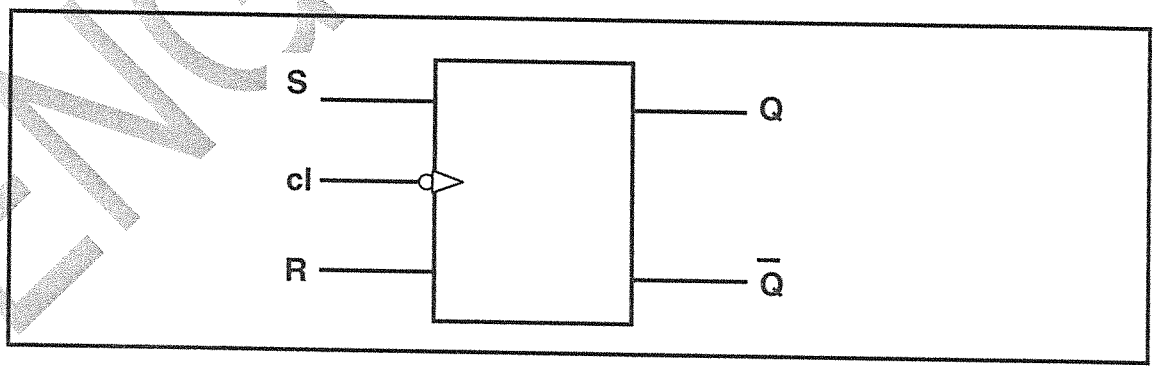

FIGURE 2

3.2.1 What type of flip-flop is represented in FIGURE 2 above? (2)

3.2.2 Draw the truth table for the flip-flop in QUESTION 3.2.1 above. (3)

3.2.3 Draw the logic circuit for the IEC symbol in FIGURE 2 above. (10)
[25]

QUESTION 4

4.1 How many clock pulses does it take to load a 4-bit number into each of the following:

4.1.1 a 4-bit PISO (parallel-in-serial-out) shift register

4.1.2 a 4-bit SIPO (serial-in-parallel-out) shift register

(2 x 2) (4)

4.2 Draw a fully labelled circuit diagram of a shift register using D-type flip-flops with the following features: series input, parallel output and output control. (10)

4.3 Explain the difference between an *asynchronous counter* and a *synchronous counter.* (4)

4.4 Draw a neat, labelled circuit diagram of an asynchronous decimal up-counter using JK-type flip-flops. (7)

[25]

TOTAL SECTION B: 90
GRAND TOTAL: 100