higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

(8080273)

24 November 2022 (X-paper)
09:00–12:00

Calculators may NOT be used. Drawing instruments may be used.

This question paper consists of 7 pages.

209Q1E2224

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer all the questions.
2. Read all the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Start each question on a new page.
5. All sketches and diagrams must be large, clear and neat.
6. Keep questions and subsections of questions together.
7. Questions must be answered with a blue or black pen and all drawings must be drawn with a pencil.
8. All calculations must be shown.
9. Write neatly and legibly.

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QUESTION 1: NUMBER SYSTEMS

Convert each of the following numbers to its binary equivalents and then complete the calculations in the binary number system. Show all conversions.

1.1 $32{,}5_{16} + 32{,}5_{8} + 32{,}5_{10}$

Convert the final answer to the hexadecimal system.

1.2 $55{,}5_{10} \times 2{,}3_{8}$

Convert the final answer to the octal system.

1.3 $C4{,}6_{16} – 2{,}4_{8}$

Use the one's complement method and convert the final answer to the octal system.

1.4 $8C{,}4_{16} \div 5{,}4_{8}$

Convert the final answer to the decimal system.

(4 × 5) **[20]**

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS, DECODERS AND ARITHMETIC ELEMENTS

2.1 What does *ASCII* stand for? (2)

2.2 Decode the following word which is in the *ASCII* code:

011 1000
011 1110
010 0001
010 0101
101 0001 (5)

2.3 Encode or decode each of the following to the code/number system indicated:

2.3.1 174_{10} to the Gray code (3)

2.3.2 The 2421 BCD code 10111101 to its decimal equivalent (2)

2.3.3 1000 0111 XS3 (Excess 3) code to decimal (2)

2.4 Sketch the block diagram and complete the truth table for a full adder which uses two half adders and an OR gate. (6)

[20]

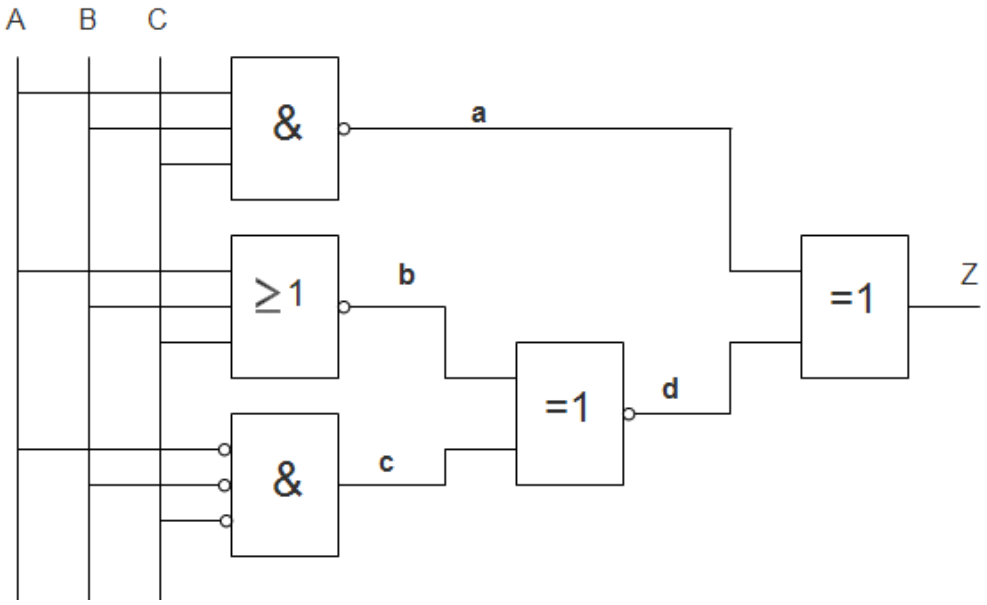
QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES

3.1 The NOR gate is a commonly used gate.

3.1.1 Draw and fully label the switch circuit for a NOR gate. (3)

3.1.2 Sketch the IEC symbol for a NOR gate. (1)

3.2 Given below is a circuit diagram that consists of logic gates.



Copy and complete the truth table for the circuit:

A	B	C	a	b	c	d	Z
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

(5)

3.3 Make a neat, labelled sketch of the circuit diagram of the following Boolean expression without changing or simplifying the expression:

$$F = \overline{A\overline{B} + \overline{\overline{A} + \overline{B}} + \overline{AB + C}}$$ (5)

3.4 Define the following logic gates:

3.4.1 An inclusive OR gate

3.4.2 A NAND gate

3.4.3 An inverter

(3 × 2) (6)

[20]

QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 Define *a latch* as used in digital electronics. (1)

4.2 Draw the truth table of a clocked RS flip-flop (4)

4.3 Name TWO types of flash memory devices. (2)

4.4 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (4.4.1–4.4.5) in the ANSWER BOOK.

4.4.1 A major disadvantage of the mask ROM:

A Very expensive to change stored data when system requirements change
B Time consuming to change stored data when system requirements change
C Extremely short life expectancy and requires frequent replacement
D Cannot be reprogrammed if stored data must be changed

4.4.2 How can UV-erasable PROMs be recognised?

A It will have a small violet dot next to the #1 pin.
B There is a small window on the chip.
C Its part number always starts with a U such as U12.
D It is not readily identifiable as it must always be kept under a small cover.

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4.4.3 Why is a refresh cycle necessary for dynamic RAM?

A The refresh cycle keeps the charge on the capacitor cells.
B The refresh cycle sets the flip-flops.
C The refresh cycle clears the flip-flops.
D The refresh cycle discharges the capacitor cells.

4.4.4 A J-K flip-flop is in a “no change” condition when …

A J =1, K = 1
B J =1, K = 0
C J = 0, K = 1
D J = 0, K = 0

4.4.5 Dynamic memory …

A must be refreshed periodically or it will lose storage.
B will maintain storage even if power is removed.
C consists of a flip-flop without a capacitive element.
D contains data that can never be altered.

(5 × 1) (5)

4.5 Explain the meaning of each of the following with regard to clock inputs of a flip-flop:

4.5.1 Small circle on the clock input.

4.5.2 A clock input without a circle

(2 × 2) (4)

4.6 Explain what you understand by *combinational logic circuit.* (2)

4.7 What is the meaning of the following pulses as used by flip-flops:

4.7.1 SD

4.7.2 RD

(2 × 1) (2)

[20]

QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1 Indicate whether the following statements are TRUE or FALSE by writing only 'True' or 'False' next to the question number (5.1.1–5.1.3) in the ANSWER BOOK.

5.1.1 An asynchronous counter differs from a synchronous counter in the method of clocking.

5.1.2 An example of an asynchronous counter is a ripple counter.

5.1.3 Bidirectional shift registers can shift data either right or left.

(3 × 1) (3)

5.2 Draw a fully labelled diagram of module 7 counter using JK flip-flops and logic gates. (6)

5.3 Choose a term from COLUMN B that matches a description in COLUMN A. Write only the letter (A–G) next to the question number (5.3.1–5.3.5) in the ANSWER BOOK.

COLUMN A	COLUMN B
5.3.1 Time required to change the pulse from 90% to 10% of its maximum.	A Switch-on time
5.3.2 The time which elapses from the time the input pulse reaches 10 % of its maximum until the output signal has reached 10 % of its maximum.	B Delay time
5.3.3 The time which elapses from the time the input signal first reaches 10 % of its maximum until the output signal first reaches 90 % of its maximum.	C Rising time
5.3.4 The time which elapses from the time the input pulse reaches 90 % of its maximum to the time the output pulse reaches 90 % of its maximum.	D Switch-off time
5.3.5 Time required to change the pulse from 10% to 90% of its maximum.	E Storing-time
	F Falling time
	G Holding time

(5 × 1) (5)

5.4 Draw a fully labelled diagram of a synchronous decade counter using JK flip-flops. (6)

[20]

TOTAL: 100