

higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

**T860(E)(N19)T
NOVEMBER EXAMINATION**

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

(8080273)

**19 November 2014 (Y-Paper)
13:00–16:00**

Calculators may NOT be used.

This question paper consists of 8 pages.

DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA
NATIONAL CERTIFICATE
LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
 2. Read ALL the questions carefully.
 3. Number the answers according to the numbering system used in this question paper.
 4. Write neatly and legibly.
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SECTION A**QUESTION 1**

1.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (1.1.1–1.1.10) in the ANSWER BOOK.

1.1.1 In positive logic, logic gate 1 corresponds to ...

- A positive voltage.
- B higher voltage level.
- C zero voltage level.
- D lower voltage level.

1.1.2 The output of a 2-input OR gate is 0 only when ...

- A both inputs are 0.
- B either input is 1.
- C both inputs are 1.
- D either input is 0.

1.1.3 The two's complement of 1000_2 is:

- A 0111
- B 0101
- C 1000
- D 0001

1.1.4 An output of full adder is in the form of ...

- A sum.
- B carry.
- C sum and carry.
- D difference.

1.1.5 8421 codes are also known as:

- A Gray code
- B ASCII code
- C Excess 3 code
- D BCD code

1.1.6 A single transistor can be used to build one of which following digital logic gates?

- A AND gates
- B OR gates
- C NOT gates
- D NAND gates

- 1.1.7 Which statement BEST describes the operation of a negative-edge-triggered D flip-flop?
- A The logic level at the *D* input is transferred to *Q* on negative of *clock*
 - B The *Q* output is ALWAYS identical to the clock input if the *D* input is HIGH
 - C The *Q* output is ALWAYS identical to the *D* input when the clock is positive
 - D The *Q* output is ALWAYS identical to the *D* input
- 1.1.8 A J-K flip-flop is in a “no change” condition when ...
- A $J = 1, K = 1$
 - B $J = 1, K = 0$
 - C $J = 0, K = 1$
 - D $J = 0, K = 0$
- 1.1.9 On the third clock pulse, a 4-bit Johnson sequence is $Q_0 = 1, Q_1 = 1, Q_2 = 1$, and $Q_3 = 0$. On the fourth clock pulse, the sequence is ...
- A $Q_0 = 1, Q_1 = 1, Q_2 = 1, Q_3 = 1$
 - B $Q_0 = 1, Q_1 = 1, Q_2 = 0, Q_3 = 0$
 - C $Q_0 = 1, Q_1 = 0, Q_2 = 0, Q_3 = 0$
 - D $Q_0 = 0, Q_1 = 0, Q_2 = 0, Q_3 = 0$
- 1.1.10 Which is the type of memory for information that does not change on your computer?
- A RAM
 - B ROM
 - C ERAM
 - D RW/RAM

(10 × 1) (10)

1.2 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (1.2.1–1.2.9) in the ANSWER BOOK.

- 1.2.1 ASCII is an abbreviation for the American Standard Convention for Intelligent Interchange. (1)
- 1.2.2 Master/slave *J-K* flip-flops are called pulse-triggered or level-triggered devices because input data is read during the entire time the clock pulse is at a LOW level. (1)
- 1.2.3 ROMs are used to store data that generally cannot be easily changed. (1)
- 1.2.4 Parallel load means to load all flip-flops at the same time. (1)

- 1.2.5 A universal shift register has both serial and parallel input and output capacity. (1)
- 1.2.6 64 hexadecimal equals 100 decimal. (2)
- 1.2.7 If you borrow from a position that contains a 0, you must borrow from the more significant bit that contains a 1. All 0s up to that point become 1s, and the digit last borrowed from becomes a 0. (1)
- 1.2.8 If both inputs are required to be ON for the output to be OFF, the gate must be an AND gate. (1)
- 1.2.9 A negative edge-triggered flip-flop will accept inputs only when the clock is LOW. (1)

- 1.3 Choose an item/a word from COLUMN B that matches a description in COLUMN A. Write only the letter (A–E) next to the question number (1.3.1–1.3.5) in the ANSWER BOOK.

COLUMN A		COLUMN B
1.3.1	It is the time which elapses from the time the input signal first reaches 10% of its maximum until the output signal first reaches 90% of its maximum.	A rising time
1.3.2	It is the time which elapses from the time the input pulse reaches 10% of its maximum to the time the output pulse reaches 10% of its maximum.	B falling time
1.3.3	It is the time required for the pulse to rise from 10 to 90% of its maximum.	C delay time
1.3.4	It is the time required for the pulse to drop from 90 to 10% of its maximum.	D storing time
1.3.5	It is the time which elapses from the time the input pulse reaches 90% of its maximum to the time the output pulse reaches 90% of its maximum.	E switch-on time

(5 × 1)

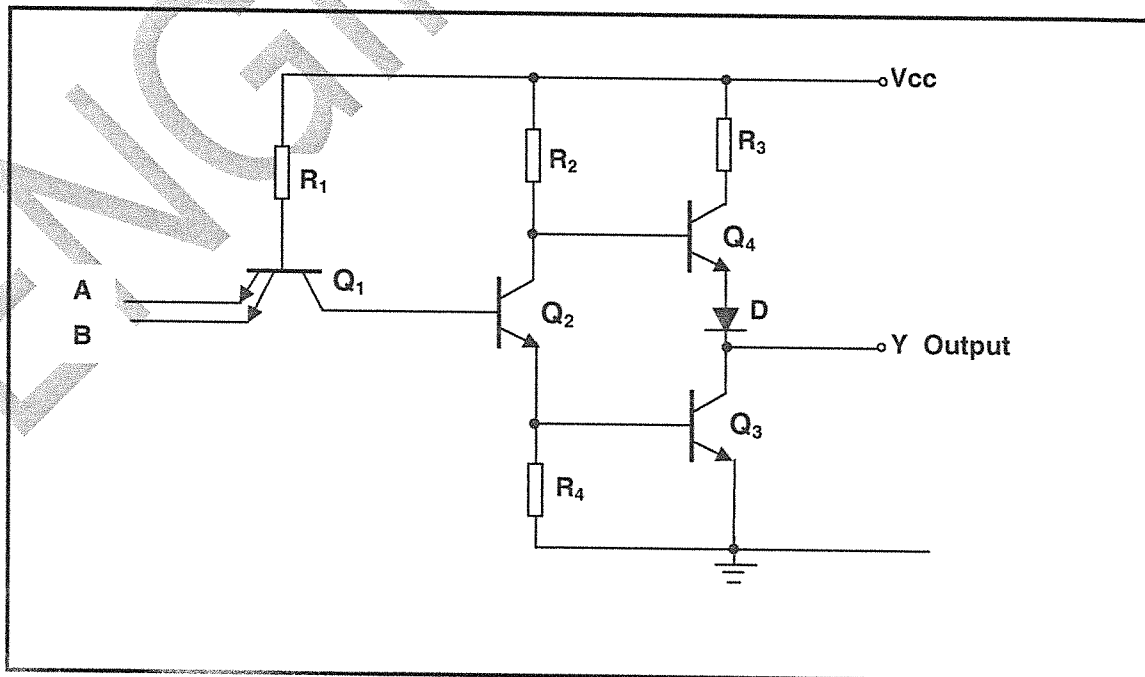
(5)
[25]**TOTAL SECTION A: 25**

SECTION B**QUESTION 2**

- 2.1 Draw a logic circuit for a full subtractor. (5)
- 2.2 Complete the following calculations in the binary number system and then follow the instruction in brackets:
- 2.2.1 $18_{16} \times 111_2$ (convert the answer to octal number system)
- 2.2.2 $124_8 \div 1100_2$ (convert the answer to hexadecimal)
- 2.2.3 $100_{10} - 40_{16}$ (use of two's complement) (3 x 4) (12)
- 2.3 Use the Hamming code to add parity bits to this word 1000 before it is ready for transmission. (5)
- 2.4 Draw a logic circuit for a 2421 BCD encoder. (6)
- 2.5 Convert the binary number 11011000 to 4221 BCD decimal equivalent. (2)
- [30]

QUESTION 3

- 3.1 Study and analyse FIGURE 1 below and answer the questions.

**FIGURE 1**

- 3.1.1 Complete the truth table below in the ANSWER BOOK by making use of FIGURE 1 on page 6.

A	B	Q ₁	Q ₂	Q ₃	Q ₄	D	Y
OFF	OFF						
OFF	ON						
ON	OFF						
ON	ON						

(10)

- 3.1.2 Identify the name of the gate represented in FIGURE 1 above. (2)

- 3.2 Draw the switch circuit for a TWO input XOR gate. (3)
[15]

QUESTION 4

- 4.1 FIGURE 2 below is an IEC symbol for a clocked J-K flip-flop. Study it and answer the questions.

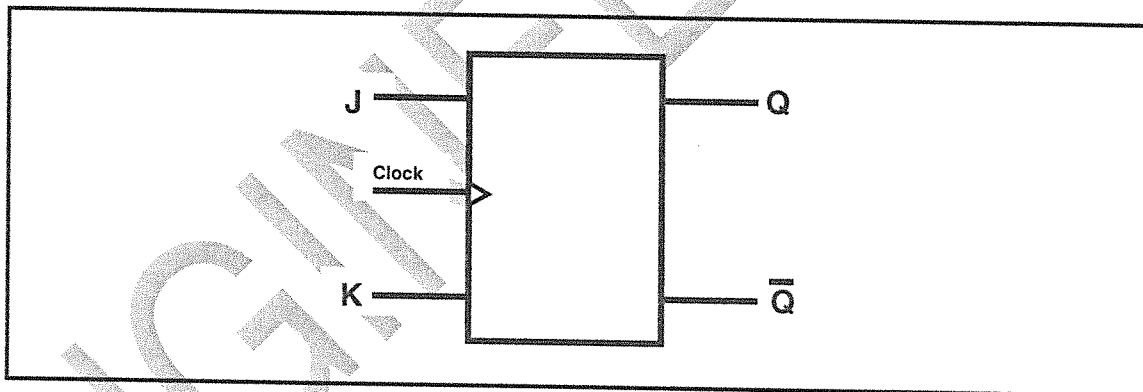


FIGURE 2

- 4.1.1 What is a flip-flop? (2)

- 4.1.2 Write the truth table for FIGURE 2 above that is triggered by the positive-going edge of the clock signal. (4)

- 4.1.3 Redraw and complete FIGURE 3 below in the ANSWER BOOK with the following conditions:

Initially all inputs are zero and assume the 'Q' output to be 1.

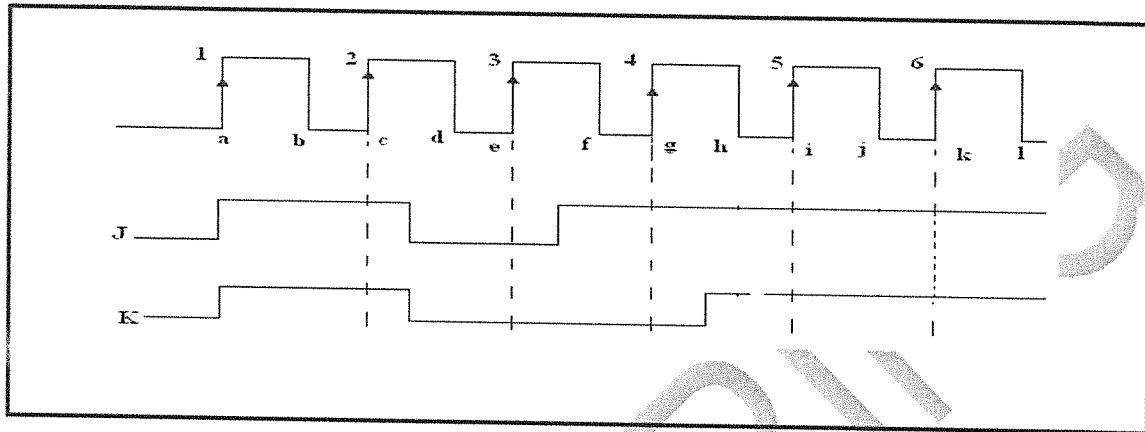


FIGURE 3

(4)

- 4.2 ROM is a class of storage medium used in computers and other electronic devices.

4.2.1 What is ROM?

(2)

4.2.2 Is ROM a volatile memory? Explain.

(1 x 2)

(3)
[15]

QUESTION 5

5.1 What are the THREE functions of a shift register?

(6)

5.2 Draw a series-in, series-out shift register consisting of four D-type master slave flip-flops.

(5)

5.3 Draw the timing diagram of a synchronous decade up-counter.

(4)

[15]

TOTAL SECTION B: 75
GRAND TOTAL: 100