higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T930**(E)**(A1)T

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

(8080273)

1 August 2018 (X-Paper)
09:00–12:00

Calculators may NOT be used.

This question paper consists of 8 pages.

DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Keep questions and subsections of questions together.
5. ALL the sketches and diagrams must be large, clear and neat.
6. Show ALL the steps and calculations.
7. Write neatly and legibly.

QUESTION 1: NUMBER SYSTEMS AND ARITHMETIC ELEMENTS

Convert each of the following numbers to their BINARY equivalents, then complete the calculations in the binary number system and then follow the instruction. Show ALL the conversions.

1.1 $14,5_{10} + 4,6_8 + 3,F_{16}$

Convert the final binary answer to the octal number system.

1.2 $31,F_{16} - 31,2_8$

Make use of the one's complement method and convert the final binary answer to the decimal number system.

1.3 $6E,1_{16} \times 3,25_{10}$

Convert the final binary answer to the hexa-decimal number system.

1.4 $A8, 7_{16} \div 13, 75_{10}$

Convert the final binary number answer to the decimal number system.

(4 × 5) **[20]**

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS AND DECODERS

2.1 What is a parity bit used for? (2)

2.2 What is the function of an encoder? (2)

2.3 If a 2421 BCD decoder can only count up to 9, why does it have 10 output lines? (2)

2.4 Encode the following to the code as indicated:

2.4.1 361_{10} to the excess-3 code

2.4.2 10011101 Gray to the 8421 BCD code

(2 × 3) (6)

2.5 The following word is received at the end of a transmission data line:

1 1 1 0 1 0 1 1
1 1 0 1 1 1 0 0
1 0 1 1 1 1 0 1
1 0 0 1 0 0 1 1
1 1 1 1 0 0 1 1
1 1 0 0 1 0 1 0

By using even parities, determine whether any faults occurred during the transmission and if so, rectify the fault/s. (8)
[20]

QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES

3.1 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (3.1.1–3.1.5) in the ANSWER BOOK.

3.1.1 An exclusive-NOR gate output is HIGH when the inputs are unequal.

3.1.2 As a rule, CMOS has the lowest power consumption of all the IC families.

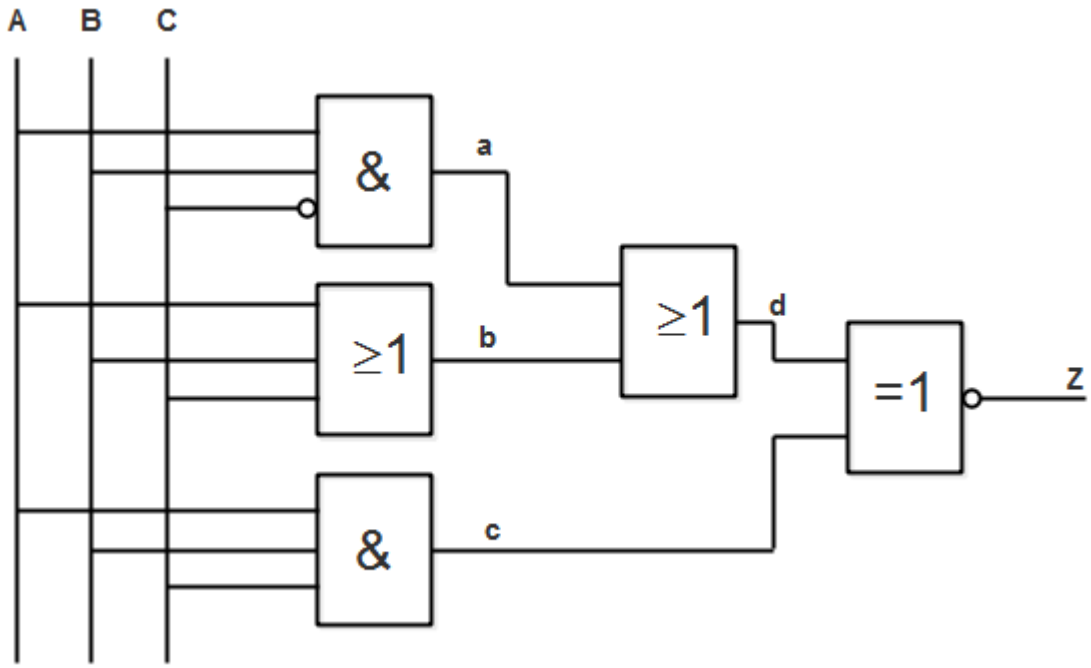
3.1.3 Power is connected to pins 7 and 14 of a 7408 quad two-input AND gate IC to allow voltage for all four AND gates on the IC.

3.1.4 The output of an AND gate with three inputs, A, B, and C, is HIGH when A = 1, B = 1, C = 1.

3.1.5 The output of a NOT gate is HIGH when the input is HIGH.

(5 × 1) (5)

3.2 The following circuit diagram consists of AND gates, OR gates and an XNOR gate:



Copy and complete the truth table for the circuit in your ANSWER BOOK.

A	B	C	a	b	c	d	Z
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

(5)

3.3 Make a neat, labelled sketch of the circuit diagram of the Boolean expression below without changing or simplifying the expression.

$Z = \overline{AC} + \overline{AB} + (A\bar{B}C.\ ABC)$ (5)

3.4 Show, by means of a circuit diagram, how diodes can be used to construct an OR gate. (5)

[20]

QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (4.1.1–4.1.5) in the ANSWER BOOK.

4.1.1 Select the statement that best describes Read-Only Memory (ROM).

A Non-volatile, used to store information that changes during system operation
B Non-volatile, used to store information that does not change during system operation
C Volatile, used to store information that changes during system operation
D Volatile, used to store information that does not change during system operation

4.1.2 What is the major difference between SRAM and DRAM?

A DRAM's must be periodically refreshed.
B SRAM's can hold data via a static charge, even with the power off.
C The only difference is the terminal from which the data is removed - from the FET drain or source.
D Dynamic RAM's are always active while static RAM's must reset between data read/write cycles.

4.1.3 Which type of ROM has to be custom-built by the factory?

A ROM
B Mask ROM
C EPROM
D EEPROM

4.1.4 The mask ROM is … technology.

A MOS
B diode
C resistor-diode
D DROM

4.1.5 An 8-bit address code can select … locations in memory.

A 8
B 256
C 65,536
D 131,072

(5 × 1) (5)

4.2 What is the advantage of using CD-RW over CD-R? (2)

4.3 Memories are divided into two groups, namely main memories and secondary memories.

Copy and complete the following table in your ANSWER BOOK by filling in TWO examples of each memory:

MAIN MEMORY	SECONDARY MEMORY

(2 × 2) (4)

4.4 Explain the following terms with respect to a timing diagram:

4.4.1 Holding time

4.4.2 Edge-triggering

4.4.3 Rising time

(3 × 2) (6)

4.5 What are *flash memories*? (3)
[20]

QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (5.1.1–5.1.5) in the ANSWER BOOK.

5.1.1 A serial in/parallel out, 4-bit shift register initially contains all 1's. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains …

A 0000.
B 1111.
C 0111.
D 1000.

5.1.2 How many clock pulses will be required to completely serially load a 5-bit shift register?

A 2
B 3
C 4
D 5

5.1.3 What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?

A Parallel-in, parallel-out
B Parallel-in, serial-out
C Serial-in, parallel-out
D Serial-in, serial-out

5.1.4 How many flip-flops are required to make a MOD-32 binary counter?

A 3
B 45
C 5
D 6

5.1.5 Which segments of a seven-segment display would be required to be active to display the decimal digit 2?

A a, b, d, e, and g
B a, b, c, d, and g
C a, c, d, f, and g
D a, b, c, d, e, and f

(5 × 1) (5)

5.2 A parallel-in series-out shift register is a register where the parallel input is connected to the pre-set (SD) and pre-set (RD) inputs of the flip-flop.

Draw the circuit of a parallel-in series-out shift register. (10)

5.3 Two counters are being used, the synchronous and the asynchronous counters.

State which counter is faster and explain why it is faster. (3)

5.4 State TWO advantages of using a JK flip-flop instead of a D flip-flop when designing shift registers and counters. (2)

[20]

TOTAL: 100